

MOS STATIC RAM

This invention relates to a MOS static RAM (random access memory).

A memory cell in an MOS static RAM has, for example, a static type flip-flop circuit comprising of a pair of driving MOSFETs whose gates and drains are mutually cross-coupled, a load element, and a pair of transfer gate MOSFETS. A memory array is then formed by a plurality of such memory cells arranged in a matrix and a plurality of complementary data line pairs to which are connected input-output terminals of corresponding memory cells. The load element may be, for example, an MOSFET which is steadily turned on, and is interposed between each complementary data line and the power terminal of the circuit.

15 A RAM having a structure in which the load resistors are connected to the data lines, is shown, for example, in U.S. Patent Specification No. 4,272,834.

The load resistors connected to the complementary data lines operate so that the potential of the complementary data lines is set to a predetermined potential before a data read-out operation from the memory cells and before a data write-in operation into them. The access time of the memory in the data read-out and write-in operations can be made constant by the pre-setting of the potential of the complementary data lines.

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As a result of studies, however, the inventors of the present invention have found that the following problems occur when fixed resistance loads constituted by MOSFETs described above are used.

5 In the data read-out operation, a predetermined word line is selected, thereby selecting a certain memory cell. Then, the level of a pair of complementary data lines is determined by the selected memory cell. In this case, the read-out low level of one of the complementary data lines is
10 determined by the ratio of the conductance characteristics of the driving MOSFETs and transfer gate MOSFETs to the conductance characteristics of the load MOSFETs. When a plurality of memory cells are selected sequentially in order to read out the data (stored information) stored in a
15 plurality of memory cells continuously, the levels of the complementary data lines are sequentially determined by the selected memory cells. In this case, if data of the opposite level is read out such as when the stored information of a logic "1" is read out after the read-out of
20 the stored information of a logic "0", for example, the levels of the complementary data lines change greatly from the high and low levels to the low and high levels, respectively. Here, the speed of the change of level of each complementary data line is limited by non-negligible
25 capacitance which is formed by parasitic capacitance and stray capacitance coupled to the complementary data lines. As a result, the data read-out speed is restricted.

The inventors of the present invention have observed that when the level change width of each of the complementary data lines is reduced, the time of the change from one level to the other can be reduced, that the charge-up speed to the complementary data lines can be increased by increasing the conductance of the load MOSFETs and the level change width of the complementary data lines can be reduced, as well. Therefore, the inventors have examined the possibility of increasing the conductance of the load MOSFETs as much as possible in order to achieve high speed in the read-out operation.

It has been found, however, that a further problem develops, namely that the read-out operation is substantially effected for a memory cell which is coupled to the unselected complementary data lines in the write-in operation and which is selected by the word line. Therefore, if the conductance of the load MOSFETs are increased, relatively large currents flow between the load MOSFETs and the selected memory cells. A current flowing between the memory cell coupled to the unselected complementary data line and the load MOSFET is irrelevant to the write-in data; hence, it is a kind of a wasteful current. However, the read-out speed will be reduced if the conductance characteristics of the load MOSFETs are reduced in order to reduce this wasteful current.

The present invention seeks to overcome this problem. It does this by providing an MOS static RAM comprising:

a plurality of static memory cells;

a pair of complementary data lines to which data input-output terminals of the static memory cells are connected;

a plurality of word lines to which the selection terminals of the static memory cells are connected, respectively;

variable load means between a power terminal of the circuit and the complementary data lines, respectively, the variable load means being adapted to be controlled such that their impedance becomes higher in a data write-in operation than the impedance thereof in a data read-out operation;

selection means for selecting one of said plurality of word lines;

control means for controlling the state of the word line in the read-out operation so that the selected state of the word line is held during a period from the start of the selection of the word line to the time when there is a predetermined difference in the level difference between the pair of complementary data lines to be changed in accordance with the data stored in the static memory cell to which the word line is coupled, the word line being brought into the unselected state after the period.

In this way it is possible to provide an MOS static
5 RAM which operates at high speed and consumes little power.

Embodiments of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing one embodiment of
10 the present invention;

Fig. 2 is a circuit diagram showing another load circuit arrangement;

Fig. 3 is a diagram useful for explaining the voltage characteristics of its read-out level; and

15 Fig. 4 is a circuit diagram showing a third load circuit arrangement.

Embodiment 1

Fig. 1 is a circuit diagram of one embodiment of the present invention. The particular configuration is not
20 essential to the invention, but as shown, a RAM is formed on one semiconductor substrate such as single crystal silicon by the well-known CMOS (complementary metal-insulator-semiconductor) integrated circuit (IC) technique.

The MOSFETs forming the memory cells are of the N-
25 channel type and are formed on P-type well regions that are in turn formed on an N-type semiconductor substrate. P-channel MOSFETs are formed on the N-type semiconductor sub-

strate. The P-type well region which acts as a substrate gate of the N-channel MOSFETs is connected to an earth terminal of a circuit, and the N-type semiconductor substrate which acts as a common substrate gate of the P-channel MOSFETs is connected to a power terminal of the circuit. A structure in which the MOSFETs constitute the memory cells in the well regions helps to prevent erroneous inversion of data stored in the memory cells, such inversion being induced by e.g. α particles.

10 Terminals A_x , A_y , D_{in} , D_{out} , $\overline{WE}$, $\overline{CS}$, V_{CC} and GND are external terminals for the integrated circuit.

A memory array M-ARY has a plurality of memory cells MC that are arranged in a matrix, word lines W_0 to W_n and complementary data lines D_0 , $\overline{D_0}$ to $\overline{D_1}$, D_1 .

15 The memory cells MC each have the same construction. As represented by one specific circuit, each memory cell MC is constructed of memory MOSFETs Q_1 and Q_2 whose gates and drains are cross-connected to each other and whose sources are connected to earth GND, and high resistance resistors R_1 and R_2 between the drains of these MOSFETs Q_1 and Q_2 and the power terminal V_{CC} , respectively, and that are comprised of a polycrystalline silicon layer. Transfer gate MOSFETs Q_3 and Q_4 are interposed between the common junctions of MOSFETs Q_1 and Q_2 and the complementary data lines D_0 and $\overline{D_0}$, respectively. The gates of the transfer gate MOSFETs Q_3 , Q_4 that are in the same row are connected in common to the corresponding word lines W_0 , W_1 and W_n as shown in the circuit diagram. The input/output terminals of the

memory cells disposed in the same column are connected to the corresponding pair of complementary data (or bit) lines D_0 and $\bar{D}_0$, D_1 and $\bar{D}_1$, and the like as also typically shown in the drawing.

5 The gate electrodes of the transfer gate MOSFETs Q_3 and Q_4 are regarded as the selection terminals of the memory cells, and the current transfer electrodes or source-drain electrodes connected to the data lines D_0 , $\bar{D}_0$ of the transfer
10 gate MOSFETs Q_3 and Q_4 are regarded as the data input/output terminals of the memory cell.

In the memory cell, though the MOSFETs Q_1 , Q_2 and the resistors R_1 , R_2 constitute a kind of flip-flop circuit, the operating point in the data retention state is different from that of flip-flop
15 circuits in the ordinary meaning of the term. That is, the resistor R_1 of the memory cell MC described above has an extremely high resistance value so that the gate voltage of MOSFET Q_2 when
20 MOSFET Q_1 is turned off is a little bit higher than the threshold voltage of Q_2 , in order to accomplish low power consumption. Similarly, R_2 , too, has an extremely high resistance value. This means that both the resistors R_1 and R_2 have high resistance
25 so that they can compensate for the drain leakage

current of MOSFETs Q_1 and Q_2 . The resistors R_1 and R_2 have a current supply capacity such that they prevent the discharge of the data charge stored in the gate capacitance (not shown) of MOSFET Q_2 . For
5 example, the drain leakage current of MOSFETs Q_1 and Q_2 is typically of the order of 10^{-12} amperes. The resistors R_1 and R_2 are of the order of about 10 giga-ohms so as to correspond to the drain leakage current.

10 In accordance with this embodiment, although RAM is produced by the CMOS-IC technique, the memory cell MC is constituted from N-channel MOSFETs and polysilicon resistance elements as described above.

The sizes of the memory cells and memory
15 array of this embodiment can be reduced when compared with the case where P-channel MOSFETs are used in place of polysilicon resistance elements. In other words, when a polysilicon resistor is used, it can be formed integrally with the gate electrode
20 of the driving MOSFET Q_1 or Q_2 , and its own size can be made compact. If a P-channel MOSFET is used, on the other hand, it must be spaced relatively far from the driving MOSFETs Q_1 and Q_2 . The use of a polysilicon resistor eliminates such unnecessary
25 space on the semiconductor substrate.

In the figure, the word line W_0 is selected by the output signal which is generated by an NOR gate circuit G_1 constituting an X address decoder X-DCR. This also applies to other word lines W_1 ,

5 ... , W_n .

The X address decoder X-DCR described above is constructed of NOR gates G_1 , G_2 , G_3 and the like that are similar to one another. Internal complementary address signals generated by an X address buffer

10 X-ADB receiving an external address signal AX consisting of a plurality of bits (that is, an address signal produced from a suitable circuit device, not shown) are applied in a predetermined combination to the input terminals of these NOR gates G_1 , G_2 , G_3 .

15 In order to prevent unnecessary power consumption at the time of the read-out operation through the memory cells, a timing signal ϕ is applied in common to these NOR gates $G_1 - G_3$, though the arrangement is not limited to this configuration. The data
20 stored in the selected memory cell is supplied to the complementary data lines by the high level (logic "1") of the timing signal ϕ , and thereafter the word line that has been selected by the read-out operation of the stored data is put into the non-
25 selected state.

The pairs of the complementary data lines D_0 , $\bar{D}_0$ and D_1 , $\bar{D}_1$ in the memory cell described above are connected to common complementary data lines CD , $\bar{CD}$ through a column switch circuit C-SW consisting of the transfer gate MOSFETs Q_{13} , Q_{14} and Q_{15} , Q_{16} for the selection of data lines, respectively. A pair of input terminals of a read-out circuit RA and a pair of output terminals of a write-in circuit WA are connected to the common complementary data lines CD , $\bar{CD}$. The read-out circuit RA delivers a read-out signal to a data output terminal D_{out} , while the write-in circuit WA receives a write-in data signal supplied from a data input terminal D_{in} . In the active state, the write-in circuit WA sends a complementary level write-in data signal to the complementary data lines CD , $\bar{CD}$.

The read-out circuit RA is controlled in operation by a control signal ϕ_r supplied from a control circuit CONT. The read-out circuit RA differentially amplifies data signals of the common complementary data lines CD and $\bar{CD}$, and sends the amplified data signal to the data output terminal D_{out} when the read-out circuit is in an operative state. When the read-out circuit is in the inoperative state, the output terminal of the read-out circuit RA is in the high impedance state or the floating state.

The write-in circuit WA is controlled in its operation by the control signal ϕ_w . When operative, the write-in circuit WA produces a complementary data signal corresponding to the input data, that is supplied to the data input terminal D_{in} , to the common complementary data lines CD, $\overline{CD}$. When the write-in circuit WA is inoperative, the pair of its output terminals are in a high impedance state or the floating state.

Selection signals Y_0 and Y_1 generated by a Y address decoder Y-DCR are applied to the gates of the MOSFETs Q_{13} , Q_{14} and Q_{15} , Q_{16} that constitute the column switch. The Y address decoder Y-DCR is constituted by NOR gates G_4 and G_5 that are similar to each other. The internal complementary address signals generated by a Y address buffer Y-ADB receiving an external address signal AY comprising of a plurality of bits (that is, an address signal produced from a suitable circuit not shown) are applied in a predetermined combination to these NOR gates G_4 , G_5 .

Upon receiving the control signals from external terminals $\overline{WE}$, $\overline{CS}$, the control circuit CONT produces the internal control timing signal ϕ and the like described above.

When a chip selecting signal applied to the external terminal $\overline{CS}$ is at the high level, that is, at a chip non-selecting level, the internal control timing signal ϕ is held at the high level in response thereto. The internal control timing signal ϕ falls to the low level when the chip selection signal is changed to the low level and a write enable signal supplied to the external terminal $\overline{WE}$ is changed to the low level, that is, when a write-in operation mode is designated. The internal timing signal ϕ changes to the low level for a predetermined period when the chip selecting signal is at the low level under the high level state of the write enable signal, and when the address signal AX is changed under the chip selection state.

A circuit for producing such a timing signal ϕ can be constituted by a suitable combination of heretofore known circuits such as address transient detection circuits, gate circuits, delay circuits, and the like.

In this embodiment, the following circuit elements form load means coupled to the pairs of complementary data lines D_0 , $\overline{D}_0$ and D_1 , $\overline{D}_1$.

N-channel MOSFETs Q_5 to Q_8 which act as fixed resistor elements are provided in the data lines D_0 - $\overline{D}_1$, respectively. N-channel MOSFETs Q_9 to Q_{12}

are connected parallel to these transistors $Q_5 - Q_8$, respectively, in order to speed up the inversion read-out operation. The MOSFETs $Q_5 - Q_8$ operate continuously when their

5 commonly connected gates and drains are supplied with the power source voltage V_{CC} . The conductance of each of these transistors $Q_5 - Q_8$ is set to be sufficiently less than the combined conductance of the data storage MOSFETs Q_1, Q_2 and the transfer

10 gate MOSFETs Q_3, Q_4 that the difference between the high level and low level of the complementary data lines, which is determined by the memory cell, becomes sufficiently great. For example, the conductance characteristics of these MOSFETs Q_5 through Q_8 are set

15 so that the high level of the complementary data lines $D_0, \bar{D}_0$ is 3.5 V and the low level is from 0.5 to 1 V so that the voltage difference ΔV may be as great as 3 V.

The lower limit of conductance or the upper

20 limit of impedance of MOSFETs $Q_5 - Q_8$ is set to values that can compensate for at least the leakage current which develops at the junction of the transfer gate MOSFETs Q_3 and Q_4 in the memory cell.

The conductance of each MOSFET formed on one semiconductor substrate by the semiconductor integrated circuit technique is determined by the ratio of its channel width W to its channel length L (i.e., W/L).

5 The ratio W/L is $5.8 \mu\text{m}/2 \mu\text{m}$ (referred hereinafter such as $5.8/2$) for MOSFETs Q_1 and Q_2 and $2.3/2$ for MOSFETs Q_3 and Q_4 of the memory cell, though the invention is not limited to these values. The ratio W/L of MOSFETs Q_5 to Q_8 is $2.3/16$, for example, is in accordance with

10 the ratios W/L of MOSFETs Q_1 to Q_4 .

Though not particularly limited to this configuration, each channel MOSFET is arranged in the enhancement mode, and has a threshold voltage of $+0.8 \text{ V}$.

15 In accordance with this embodiment, it is possible to prevent abnormal drop of the potential on the complementary data lines during a period such as the data write-in period because MOSFETs Q_5 through Q_8 are disposed. In other words, during

20 the data write-in period, the pair of data lines that are not selected by the column switch C-SW have their levels determined by the selected memory cell. If, for example, MOSFETs Q_{13} and Q_{14} constituting the column switch C-SW are

25 turned off and the word line W_0 is at the selection

level, the levels of the unselected data lines D_0 and $\bar{D}_0$ are determined by the memory cell which is coupled to the word line W_0 . Here, the memory cell itself that has the high resistance elements R_1 and R_2 such as shown in the drawing, does not substantially have a driving capacity that keeps the data lines at the high level. Therefore, unless MOSFETs Q_5 and Q_6 are provided the data line of the unselected data lines D_0 and $\bar{D}_0$ which is to be set to the high level is substantially in the floating state. If the data lines D_0 and $\bar{D}_0$ are kept in the unselected state for a relatively long period during the write-in period in response thereto, therefore, the level of the data line of them which is to be kept at the high level is reduced abnormally by the leakage current. When MOSFETs Q_5 and Q_6 are provided as shown in the drawing, however, this abnormal drop of the complementary data line potential can be prevented, so that any adverse influences upon the access time to the memory cell can be avoided.

An internal control signal $\overline{WE} \text{ CS}$ produced from the control circuit CONT is applied to the gates of MOSFETs Q_9 through Q_{12} . Therefore, these transistors $Q_9 - Q_{12}$ are turned off only during

the write-in operation (that is, when both the chip selection signal $\overline{CS}$ and the write enable signal $\overline{WE}$ are at the low level) because the control signal $\overline{WE CS}$ is at the low level only at that time. The MOSFETs $Q_9 - Q_{12}$ are kept ON during the read-out operation and under the chip non-selection state. MOSFETs $Q_9 - Q_{12}$ under the ON state constitute load elements to the corresponding complementary data lines in cooperation with MOSFETs $Q_5 - Q_8$. The conductance of the load element in this case is set to a value such that the level difference to be set by the selected memory cell between a pair of complementary data lines is as small as possible. For example, the value is selected so that one of the complementary data lines is at the high level of 3.5 V and the other, at the low level of 3 V so that the voltage difference ΔV may be as small as 0.5 V, at a power source voltage V_{CC} of 5 V. The conductance characteristics of MOSFETs, such as those of Q_9 , for example, are set in response to the former in consideration of the relation between the combined conductance characteristics with MOSFET Q_5 connected in parallel with Q_9 and the combined conductance characteristics of the transfer gate MOSFETs in the selected memory cell MC and the driving MOSFETs

in the ON state, and also in consideration of the level difference that is to be obtained between the complementary data lines. If MOSFETs $Q_1 - Q_4$ and $Q_5 - Q_8$ have the W/L ratios such as described
 5 above, the W/L ratio of MOSFETs Q_9 through Q_{12} is set to 16/2, though the arrangement is not limited to this value.

The level difference given to the complementary data lines during the data read-out operation
 10 is applied to the read-out circuit RA through one set of column switch MOSFETs $Q_{13} - Q_{16}$ and through the common complementary data lines CD, $\overline{CD}$. The read-out circuit RA has a differential amplification function. Therefore, the level difference
 15 between the complementary data lines necessary for the data read-out operation may be relatively small as described above.

In these embodiments, the timing ϕ described above is used in order to bring all the word lines
 20 into the unselected state after the stored data of the memory cell MC is supplied to the complementary data lines and when the chip is not being selected. The timing signal ϕ is at the low level (logic "0") during the period from the start of the selection
 25 of the word lines in the read-out operation to the

occurrence of the predetermined level difference between the corresponding complementary data lines, and during the write-in operation, and is at the high level at other periods. The reason why the word lines are brought into the unselected state by the timing signal ϕ after the completion of the read-out operation of the stored data from the memory cell MC and during the time when the chip is not being accessed is as follows. Unless a control signal such as the timing signal ϕ is used, one of a plurality of word lines is brought to the selection level by the operation of the X address decoder X-DCR when the chip is not being selected. The memory cell coupled to the word line at the selection level forms a current path between one of the pair of complementary data lines and the earthing point of the circuit. In this case, therefore, a direct current continues to flow through the load circuit comprising of MOSFETs Q_5 , Q_9 and the like that are turned ON, the transfer gate MOSFETs of the selected memory cell MC, and the data storage MOSFETs that are turned ON, and wasteful current increases.

When all the word lines are brought into the non-selection level by the timing signal ϕ as in this embodiment, all the memory cells are also brought

into the unselected state in response thereto, so that the increase of the wasteful current such as described above can be prevented.

In this embodiment, since the read-out level of the complementary data lines is reduced to a minimum necessary level during read-out by reducing relatively the impedance of the load circuit of the data lines (or by increasing the conductance characteristics), the inversion read-out can be done at high speed. The level of the complementary data lines in the previous operation can be reset at a high speed by reducing relatively the impedance of the load circuit during the chip selection period, and hence the next read-out operation can be made rapidly. At this time, since the timing signal ϕ prevents the occurrence of the wasteful current, low power consumption can be accomplished.

In the write-in operation, on the other hand, the high and low levels are applied from the write-in circuit WA to the selected complementary data lines, but the low level of the data lines can be reduced to a lower potential by increasing the impedance of the load circuit. This makes it possible to execute the write-in operation at a higher speed. Since the impedance of the load circuit is increased in

this case, the wasteful current flowing through all of the remaining memory cells MC coupled to the unselected complementary data lines can be reduced. Therefore, lower power consumption can
 5 also be accomplished.

The write-in operation can be made at an arbitrary timing by the write enable signal $\overline{WE}$. Therefore, when the write-in operation is necessary, it is not suitable to employ the method which brings
 10 the word lines into the unselected state after the passage of a predetermined period from the start of selection to the completion of the read-out operation of the stored data of the memory cell MC, as in the read-out operation, thereby reducing re-
 15 quired power.

The control signal $\overline{WE} \cdot \overline{CS}$ applied to the gates of MOSFETs Q_9 through Q_{12} is changeable. These MOSFETs $Q_9 - Q_{12}$ may also be controlled, for example, by a control signal $\overline{WE} \cdot CS$ which represents the com-
 20 bination of the chip selection signal CS with the write enable signal $\overline{WE}$. When this control signal $\overline{WE} \cdot CS$ is used, MOSFETs $Q_9 - Q_{12}$ are turned ON in the chip selecting state (that is $\overline{CS}$: low level), and the read-out operation mode (that
 25 is, $\overline{WE}$: high level). Even when the control signal

is thus changed, it is possible to obtain the signal level difference necessary for the data lines at the time of read-out and write-in operations. The power consumption does not substantially change.

- 5 However, when the control method of MOSFETs $Q_9 - \bar{Q}_{12}$ is changed in this manner, it is to be noted that the access time of the memory unavoidably becomes relatively longer.

- For example, when the chip selection signal
- 10 $\overline{CS}$ is brought to the non-selecting level after the execution of the data write-in operation, MOSFETs $Q_9 - Q_{12}$ are kept OFF in the same way as in the data write-in operation. In this case, the data line that has been set in advance to the
- 15 low level by the memory cell among a plurality of data lines starts changing to the initialize level of the high level due to MOSFETs $Q_5 - Q_8$. However, the changing speed of the low level data line is greatly limited by the parasitic capacitance of
- 20 each data line and by the small conductance of MOSFETs $Q_5 - Q_8$. As a result, each data line is not always at a satisfactory initialize level when the chip is first accessed for a data read-out operation. A satisfactory initialize level is
- 25 ensured for the first time by the ON operation of

MOSFETs Q_9 through Q_{12} when the chip is first accessed for a data read-out operation.

When the control signal $\overline{WE \cdot CS}$ is used as in this embodiment, MOSFETs $Q_9 - Q_{12}$ are turned ON when chip accessing stops. Therefore, each data lines is set to the satisfactory initialize level when the chip is not being accessed; hence, rapid read-out becomes possible.

Embodiment 2

Fig. 2 is a circuit diagram showing another example of the data line load circuit in the memory array. Circuits not shown in Fig. 2 are substantially the same as those shown in Fig. 1.

In this embodiment, a series circuit comprising a P-channel MOSFET Q_{18} (Q_{20}) and an N-channel MOSFET Q_{17} (Q_{19}) is connected in parallel with the load circuit shown in Fig. 1 in order to improve the power source dependency characteristics of the read-out level (ΔV). The power source voltage V_{CC} is applied constantly to the gate and drain of the N-channel MOSFET Q_{17} (Q_{19}) in the same way as in the embodiment shown in Fig. 1. Since the internal control signal $\overline{WE \cdot CS}$ is applied to the gate of the P-channel MOSFET Q_{18} (Q_{20}), this transistor is

turned ON during the read-out operation and the chip unselected prerioid and is turned OFF during the write-in operation in the same way as the N-channel MOSFET Q_9 (Q_{10}).

5 Next, the purpose and the construction of such a series circuit of MOSFETs Q_{18} (Q_{20}) and Q_{17} (Q_{19}) will be explained.

The combined conductance (impedance) of the N-channel MOSFETs Q_5 and Q_9 (Q_6 , Q_{10}) that are
 10 turned on by the power source voltage V_{CC} and the control signal $WE \cdot CS$ formed by the power source voltage V_{CC} is relatively great; hence, the combined conductance can be regarded as keeping substantially a constant value irrespective of the drop of the power
 15 source voltage V_{CC} . In contrast, the driving MOSFET Q_1 (Q_2) and the transfer gate MOSFET Q_3 (Q_4) of the memory cell MC are dropped with those gate voltage in response to the drop of the power source voltage
 V_{CC} , so that their conductance reduces relatively
 20 greatly. For this reason, the level of the data line to be set to the low level between the complementary data lines D_0 and $\bar{D}_0$ rises toward the high level as represented by broken line in the power source voltage characteristic diagram of Fig. 3 because
 25 the ratio of conductance of the load circuit to

that of the memory cell changes when the power source voltage V_{CC} drops. As a result, the level difference (ΔV) imported to the complementary data lines D_0 and $\bar{D}_0$ by the memory cell, becomes small, and the margin of the read-out level deteriorates.

The decrease of the voltage difference between the data lines due to such an undesirable change of the conductance ratio can be substantially prevented by MOSFETs Q_{17} and Q_{18} .

The P-channel MOSFET Q_{18} constitutes a variable impedance element which is responsive to the change of the power source voltage V_{CC} . This transistor Q_{18} is turned ON when the control level WE.CS is brought to the low level during the read-out operation. The impedance at this time is increased because the gate-source bias voltage is reduced to small level in response to the drop of the power source voltage V_{CC} .

The N-channel MOSFET Q_{17} substantially constitutes a level shift element. The high level given to the data line D_0 is substantially limited to a value $V_{CC} - V_{th}$ limited by the threshold voltage V_{th} of MOSFET Q_{17} . The restriction of the high level of the data line D_0 provides the following advantage.

The gate-source voltage of the N-channel MOSFET

Q_{13} that constitutes the column switch C-SW shown in Fig. 1 is reduced if the signal to be transferred is at the high level. Therefore, MOSFET Q_{13} comes to possess a relatively high impedance for the high level signal that is to be transferred by the transistor. If the data line D_0 is at the high level, the transfer speed of the data signal transferred to the common data line CD through MOSFET Q_{13} becomes relatively lower.

10 If the high level of the data line D_0 is reduced to a relatively low level by MOSFET Q_{17} as described above, MOSFET Q_{13} comes to possess a relatively low impedance when it is turned ON by the selection signal Y_0 . As a result, the transfer speed of the data signal can be increased.

The level shift voltage caused by the N-channel MOSFET Q_{17} substantially increases the impedance change ratio of the P-channel MOSFET Q_{18} as the variable impedance element. Thus, the power source voltage V_{CC} is supplied to the source of MOSFET Q_{18} after its level is shifted by MOSFET Q_{17} . Therefore, when the power source voltage V_{CC} changes, the relative change ratio of the voltage applied across the source and gate of MOSFET Q_{18} becomes greater than the change ratio of the power source voltage

V_{CC} of its own. As a result, the impedance change ratio of MOSFET Q_{18} becomes greater.

In this embodiment, since a P-channel MOSFET Q_{18} (Q_{20}) whose conductance becomes smaller with the drop of the power source voltage V_{CC} is provided, compensation of the combined conductance characteristics of the load circuit becomes possible. Therefore, the read-out level (ΔV) of the memory cell MC can be kept substantially constant as represented by solid line in Fig. 3. Since MOSFETs Q_{17} and Q_{18} (Q_{19} , Q_{20}) are provided, the conductance of MOSFET Q_9 (Q_{10}) described above is set to be smaller than that of MOSFET Q_9 shown in Fig. 1.

If the memory cell in this embodiment is the same as that in the first embodiment, the W/L ratios of MOSFETs Q_5 , Q_9 and Q_{18} can assume the values of about 2.3/10, 3.3/2 and 25/2, respectively. The P-channel MOSFET Q_{18} has a threshold voltage of -0.8 V, for example. The W/L ratio of MOSFET Q_{17} as the level shift element is set to be about 67/2, for example, so that its impedance is sufficiently smaller than the impedance of MOSFET Q_{18} , though this is not particularly limited to this configuration.

In accordance with this second embodiment, the current path formed by MOSFETs Q_{17} , Q_{18} and the

current path formed by MOSFET Q_{19} are simultaneously turned ON and OFF by the control signals $WE \cdot CS$ and $\overline{WE \cdot CS}$, respectively. Both MOSFETs Q_{17} and Q_{19} are of the N-channel type and their gates are connected to their drains. In other words, both MOSFETs Q_{17} and Q_{19} are diode-connected. Therefore, MOSFET Q_9 can be eliminated by increasing the impedance of MOSFET Q_{17} . Likewise, MOSFET Q_{10} can be eliminated. However, if the MOSFETs Q_9 and Q_{10} are eliminated, the following must be taken into consideration.

Since the source potential of MOSFET Q_{18} is reduced by MOSFET Q_{17} , its impedance is increased drastically at a relatively early stage of the start of drop of the power source voltage V_{cc} . In other words, the current supplied to the data line D_0 through MOSFET Q_{18} decreases drastically with the drop of the power source voltage V_{cc} . The current path of MOSFETs Q_{17} and Q_{18} is substantially cut OFF when the power source voltage V_{cc} is substantially equal to the sum of the threshold voltages of these two transistors. Therefore, when the power source voltage V_{cc} drops, the low level of the data line D_0 determined by the memory cell drastically drops. This means that the voltage difference between the data lines D_0 and $\overline{D}_0$ increases with

a drop in the power source voltage V_{cc} .

However, the increase of the level difference between the data lines D_0 and $\bar{D}_0$ means an increase in the time of change of each data line from the high level to the low and vice versa, and means also an increase in the access time of the memory during continuous read-out operation of a plurality of data.

Therefore, when the increase of the access time of the memory cell is not desired, it is desirable to employ the MOSFETs Q_9 and Q_{10} as shown in Fig. 2. The MOSFETs Q_9 and Q_{10} form a current path even when power source voltage V_{cc} drops relatively greatly. Therefore, the MOSFETs Q_9 and Q_{10} prevent the undesirable increase of the level difference between the data lines D_0 and $\bar{D}_0$ brought forth by the change of impedance of MOSFET Q_{18} .

The circuit shown in Fig. 2 can be modified. For example, it is possible to connect directly the source of MOSFET Q_{18} to the power source terminal V_{cc} and to interpose the diode-connection MOSFET Q_{17} between the drain of Q_{18} and the data line D_0 . If this change is employed, the impedance change ratio of MOSFET Q_{18} becomes relatively small.

Embodiment 3

Fig. 4 is a circuit diagram showing still

another example of the load circuit for the data lines of the memory array described above.

In this embodiment, P-channel MOSFETs Q_{23} and Q_{24} connected in the latch form and P-channel MOSFETs Q_{21} and Q_{22} interposed between the sources of the former and the power source voltage V_{CC} are provided in place of the load MOSFETs Q_5 and Q_6 in Fig. 1, respectively. The internal control signal $\overline{WE} \cdot \overline{CS}$ is applied to the gates of MOSFETs Q_{21} , Q_{22} so that they are turned ON only in the write-in operation. The N-channel MOSFETs Q_{25} and Q_{26} are analogous to the N-channel MOSFETs Q_9 and Q_{10} in Fig. 1 or 2. However, their conductance is set to be relatively great because MOSFETs of the parallel connection are not provided.

In this embodiment, MOSFETs Q_{25} and Q_{26} are turned ON during the chip nonselection state and in the read-out operation, and the current necessary for the read-out operation is supplied to the complementary data lines D and $\overline{D}$. In the write-in operation, on the other hand, MOSFETs Q_{21} and Q_{22} are turned ON instead of these MOSFETs Q_{25} and Q_{26} . In this case, the read-out level supplied from the selected memory cell to the unselected complementary data lines is amplified by the positive feedback

operation of MOSFETs Q_{23} and Q_{24} connected as the latches. Therefore, the load MOSFET Q_{23} or Q_{24} connected to the data line on the side of the data storage MOSFET of the memory cell which is turned
 5 ON is turned OFF (enters a high impedance state), so that the occurrence of d.c. current in the unselected complementary data lines in the write-in operation can be prevented. Incidentally, since a large write-in level is supplied from the write-in
 10 circuit WA to the selected complementary data lines, latch MOSFETs Q_{23} and Q_{24} operate in accordance with its write-in level.

In this embodiment, if the conductance of Q_{21} - Q_{24} is less than the conductance of Q_{25} and Q_{26} ,
 15 a steady earth level may be applied to the gates of Q_{21} and Q_{22} instead of applying the $\overline{WE \cdot CS}$ signal. In this case, all the MOSFETs Q_{21} , Q_{22} , Q_{25} and Q_{26} are turned ON in the read-out operation, but the level of the data lines is determined by Q_{25} and
 20 Q_{26} because of the difference of conductance.

The present invention may provide the following effects.

(1) A variable impedance means may be used as the load circuit of the complementary data lines in the memory cell array, and its impedance is reduced in

the read-out operation and when the chip is not being accessed. Therefore, the difference in level of the complementary data lines due to the data stored in memory may be reduced to the minimum level necessary. Since reset of the
5 complementary data lines in the previous operation cycle may be effected at a high speed, the memory operation may be speeded up.

(2) Since a variable impedance means may be used as the load circuit for the complementary data lines in the memory
10 cell array, the impedance is increased only in the write-in operation so that any wasteful current, otherwise occurring from the unselected complementary data lines through the selected memory cell, may be reduced and hence lower power consumption may be accomplished.

15 (3) In the read-out operation of the memory cells, the word lines may be brought into the non-selection state after the read-out of the data stored in the memory cell to the complementary data lines and in the chip non-selection period, and occurrence of a wasteful current, which would
20 otherwise flow from the complementary data lines through the memory cell, can be prevented. Therefore, lower power consumption may be accomplished.

(4) Due to the synergistic effect of (2) and (3), extremely lower power consumption may be achieved.

25 Although the invention has thus been described with reference to particular embodiments thereof, the invention

is not limited thereto but can be changed or modified in various ways. For example, the memory cell may use a static flip-flop circuit having a combination of P-channel MOSFETs with N-channel MOSFETs. The load MOSFETs Q₅ to Q₈ may be
5 replaced by resistance means such as polysilicon. The precise construction of the memory cell array and the precise circuit construction of its peripheral circuit can be embodied in various forms.

MOSFETs Q₂₅ and Q₂₆ shown in Fig. 4 may be replaced
10 by MOSFETs Q₁₇ through Q₂₀ such shown in Fig. 2.

In the memory cell shown in Figs. 1 and 2, the flip-flop circuit comprising of the high resistance elements R₁, R₂ and MOSFETs Q₁, Q₂, can be replaced by a CMOS type flip-flop circuit consisting of two CMOS inverter circuits
15 whose inputs and outputs are cross-connected. In other words, the memory cell using a high resistance element (hereinafter called a "high resistance memory cell") such as those used in the foregoing embodiments can be changed to a CMOS type memory cell. A CMOS type memory cell needs low
20 power consumption in the same way as the high resistance memory cell. In a CMOS memory cell, the MOSFETs that correspond to the high resistance elements constitute active load elements. Therefore, the CMOS type memory cell has a relatively large driving capacity for the data lines that
25 are to be raised to the high level, unlike the high resistance memory. The drop of the level of the unselected data lines in the data write-in operation can therefore be sub-

stantially prevented by the CMOS type memory cell. Therefore, when the CMOS type memory cell is used, MOSFETs Q₅ through Q₈ shown in Figs. 1 and 2 may be deleted.

The present invention can be applied widely to MOS
5 static RAMs.

CLAIMS

1. An MOS static RAM comprising:

a plurality of static memory cells

a pair of complementary data lines to which data input-output terminals of the static memory cells are connected:

a plurality of word lines to which the selection terminals of the static memory cells are connected, respectively;

variable load means between a power terminal of the circuit and the complementary data lines, respectively, the variable load means being adapted to be controlled such that their impedance becomes higher in a data write-in operation than the impedance thereof in a data read-out operation;

selection means for selecting one of said plurality of word lines;

control means for controlling the state of the word line in the read-out operation so that the selected state of the word line is held during a period from the start of the selection of the word line to the time when there is a predetermined difference in the level difference between the pair of complementary data lines to be changed in accordance with the data stored in the static memory cell to which the word line is coupled, the word line being brought into the unselected state after the period.

2. An MOS static RAM according to claim 1 further



comprising; a control circuit for controlling the variable load means, each of the variable load means comprising a resistance element forming a current path between a corresponding complementary data line and the power terminal, and a first MISFET whose gate electrode is connected so as to receive the output signal of the control circuit the first MISFET being adapted to be turned on in a read-out operation thereby to form a current path between the complementary data line and the power terminal and being adapted to be turned off in the write-in operation.

3. An MOS static RAM according to claim 2, wherein each of the static memory cells comprises a pair of MOSFETs whose gate and drain electrodes are mutually cross-connected, load elements connected to the drain electrodes of the pair of MOSFETs, and a transfer gate MOSFET between the drain electrodes of the pair of MOSFETs and the complementary data line.

4. An MOS static RAM according to claim 2 or claim 3 wherein each of the load and resistance elements is a polysilicon resistance element.

5. An MOS static RAM according to claim 3, wherein each of the resistance elements has a diode-connected first MOSFET in the enhancement mode.

6. An MOS static RAM according to claim 5 which further comprises a pair of common complementary data lines and third and fourth MOSFETs between the complementary data lines and the pair of common complementary data lines,



respectively, the third and fourth MOSFETs being adapted to receive selection signals at the gate electrodes thereof, each of the third and fourth MOSFETs having a channel conductivity type which is turned on by a selection signal of a level substantially equal to the power source voltage of the circuit.

7. An MOS static RAM according to claim 6 wherein the pair of MOSFETs of each memory cell and the third and fourth MOSFETs have the same channel conductivity type.

8. An MOS static RAM according to any one of claims 2 to 5 wherein each of the variable load means further comprises a level shift element connected in series with the first MISFET, and the first MISFET has a channel conductivity type which is turned on by a gate potential of a level substantially equal to the earth potential of the circuit.

9. An MOS static RAM according to claim 8, wherein the level shift element is between the source electrode of the first MISFET and the power terminal.

10. An MOS static RAM according to claim 8 or claim 9, wherein the level shift element is a diode-connected second MOSFET.

11. An MOS static RAM according to claim 10, wherein the second MOSFET and the pair of MOSFETs of each memory cell have a channel conductivity type opposite to that of the first MISFET.

12. An MOS static RAM according to claim 8, wherein each variable load means further comprises a second MISFET which



forms a current path between the power terminal and the complementary data line in the read-out operation, the second MISFET being adapted to be turned off in the write-in operation, the second MISFET having a channel conductivity type opposite to that of the first MISFET.

13. An MOS static type RAM according to claim 12, wherein the level shift element has a diode-connected third MOSFET having a channel conductivity type opposite to that of the first MISFET.

14. An MOS static type RAM according to claim 13 further comprising a pair of common complementary data lines, and fourth and fifth MOSFETs between the complementary data lines and the common complementary data lines, respectively, the fourth and fifth MOSFETs being adapted to receive selection signals at the gate electrodes thereof, each of the fourth and fifth MOSFETs having the same channel conductivity type as that of the second and third MOSFETs.

15. An MOS static RAM according to claim 1 wherein the variable load means has first and second MOSFETs between the power terminal and said complementary data lines, respectively, the gate and drain electrodes thereof being mutually cross-connected, and third and fourth MOSFETs between the power terminal and said complementary data lines, respectively, each of the third and fourth MOSFETs being turned off in the data write-in operation and being turned on in the data read-out operation.



16. An MOS static RAM according to claim 15 which further comprises fifth and sixth MOSFETs connected in series with said first and second MOSFETs, each of said fifth and sixth MOSFETs being controlled so that it is turned on and off at substantially the same time as the third and fourth MOSFETs.

17. An MOS static RAM according to any one of the preceding claims, wherein the selection means includes an address decoder adapted to generate selection signals to be supplied to the word lines; and there is a further control means adapted to receive at least a chip selection signal, and adapted to set the output of the address decoder to a non-selection level in a chip non-selection state.

18. An MOS memory RAM substantially as herein described with reference to Fig. 1, or with reference to Fig. 1 as modified by Fig. 2 or Fig. 4.
