

**ABSTRACT**

Phase-locked oscillator arrangement.

This Sheet Has Been Replaced



An arrangement comprising:

- a variable-frequency oscillator (11) controlled by a voltage (VCD) from a capacitance (13)
- a charge pump circuit (15), which charges or discharges the capacitance (13)
- 5 - a phase detector (19) which compares the phase of a signal from a reference oscillator (21) with the phase of the output signal of the variable-frequency oscillator (11) after frequency division in a divider (17), which detector supplies an up-command signal (UP) and a down-command signal (DWN) to the charge pump circuit (15)
- a logic gate (31) which detects the simultaneously active state of the command signals
- 10 (UP, DWN) and whose output signal is applied to the phase detector (19) as a reset signal ( $\overline{RST}$ ) for this detector, after passage through a delay device (53).

In accordance with the invention the delay device comprises an annexed transistor (40e) forming a matched pair with one of the transistors (40a-40b, 40c-40d) forming the current sources of the charge pump circuit (15), and means (57, 59, 60, 62)

15 for supplying the reset signal ( $\overline{RST}$ ) when the current of the annexed transistor (40e) reaches a given fraction of its nominal current, after being turned on by the logic gate (31).

Field of use: frequency synthesizers.

Figure 2