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(21) International Application Number: PCT/US99/28536 (22) International Filing Date: 2 December 1999 (02.12.99) (30) Priority Data: 09/224,338 31 December 1998 (31.12.98) US (71) Applicant: MOTOROLA INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US). (72) Inventors: DUNN, Gregory, J.; 430 S. Evergreen Avenue, Arlington Heights, IL 60005 (US). SAVIC, Jovica; 4328 Roslyn Road, Downers Grove, IL 60515 (US). BEUHLER, Allyson; 1113 86th, Downers Grove, IL 60516 (US). ZHANG, Min-Xian; 155 Lake Drive South, Algonquin, IL 60102 (US). SIMONS, Bverett; 1330 West St. James Court, Palatine, IL 60067 (US). (74) Agents: FEKETE, Douglas, D. et al.; Motorola Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).		(81) Designated States: JP, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>
(54) Title: PHOTODEFINED INTEGRAL CAPACITOR WITH SELF-ALIGNED DIELECTRIC AND ELECTRODES AND METHOD THEREFOR (57) Abstract A method for manufacturing a microelectronic assembly to have aligned conductive regions and dielectric regions, for example, for producing integral capacitors (32), generally entails providing a substrate (10) with a first conductive layer (12), forming a dielectric layer (14) on the first conductive layer, and then forming a second conductive layer on the dielectric layer (16). A first region of the second conductive layer is then removed to expose a first region of the dielectric layer, which in turn is removed to expose a first region of the first conductive layer that is also removed. From this process, the first regions of the conductive and dielectric layers are each removed by using the overlying layer or layers as a mask, so that the remaining second regions of these layers are coextensive.		