1. A device comprising:

a transistor having a gate on a substrate, the gate includes a gate electrode over a gate dielectric;

a gate dielectric protection module coupled to the transistor, wherein the gate dielectric protection module, when activated, provides a protection bias to reduce a voltage difference between the gate and substrate (V_{DIFF}) to below a breakdown voltage (V_{BD}) of the gate dielectric.

2. The device of claim 1 wherein:

the transistor includes a transistor body in the substrate; and

the gate dielectric protection module is coupled to the transistor body.

3. The device of claim 2 wherein the gate dielectric protection module provides the protection bias to the transistor body to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} to at least 5% below V_{BD}.

4. The device of claim 1 wherein the gate dielectric protection module provides the protection bias to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} below V_{BD}.

5. The device of claim 1 wherein the gate dielectric protection module provides the protection bias to reduce V_{DIFF} to at least 5% below V_{BD}.

6. The device of claim 1 wherein the gate protection module comprises:

a sensing circuit for detecting an ESD event; and

a biasing circuit coupled to the transistor,

wherein the sensing circuit activates the biasing circuit when an ESD event is detected to provide the protection bias.

7. The device of claim 6 wherein the sensing circuit comprises:

a sensing resistor coupled in series with a sensing capacitor disposed between first and second rails, wherein the sensing resistor is coupled to the first rail and the sensing capacitor is coupled to the second rail; and

a sensing circuit output coupled to the biasing circuit, the sensing circuit output is disposed between a common terminal of the sensing resistor and sensing capacitor, wherein the sensing circuit generates an inactive sensing output signal at the sensing circuit output when no ESD event is detected and an active sensing output signal when an ESD event is detected to activate the biasing circuit.

8. The device of claim 7 wherein the biasing circuit comprises:

first and second transistors coupled in series between the first and second rails, a first terminal of the first transistor is coupled to the first rail and a first terminal of the second transistor is coupled to the second rail;

a biasing input coupled to gates of the first and second transistors; and

a biasing output coupled to common second terminals of the first and second transistors.

9. The device of claim 8 wherein:

the first rail is a high power rail;

the second rail is a ground rail;

the first biasing transistor is a p-type transistor;

the second biasing transistor is a n-type transistor; and

when the protection circuit is activated, the first biasing transistor is switched on and the second biasing transistor is switched off to allow current to flow from the first rail to the biasing output through the first transistor.

10. The device of claim 9 wherein the current at the biasing output flows to the body of the transistor to produce the protection bias to reduce V_{DIFF}.

11. The device of claim 9 comprises:

a biasing output resistor coupled to the biasing output and the second rail, wherein the current at the biasing output flows through the resistor to produce the protection bias to reduce V_{DIFF}.

12. The device of claim 6 wherein:

the transistor is part of an I/O cell coupled to an I/O pad;

the I/O cell includes an I/O transistor coupled in series with the transistor between first and second rails, the first terminal of the I/O transistor is coupled to the first rail and the first terminal of the transistor is coupled to the second rail;

an I/O cell input couples the I/O pad to gates of the I/O transistor and the transistor; and

an I/O cell output is coupled to common second terminals of the I/O transistor and the transistor.

13. The device of claim 12 wherein:

the I/O transistor is a p-type transistor;

the transistor is a n-type transistor;

the first rail is a high power rail; and

the second rail is a ground rail.

14. The device of claim 6 comprises a rail based ESD protection circuit coupled to the transistor.

15. The device of claim 6 comprises a pad based ESD protection circuit coupled to the transistor.

16. A method for forming a device comprising:

forming a transistor having a gate on a substrate, the gate includes a gate electrode over a gate dielectric; and

forming a gate dielectric protection module coupled to the transistor, wherein the gate dielectric protection module, when activated, provides a protection bias to reduce a voltage difference between the gate and substrate (V_{DIFF}) to below a breakdown voltage (V_{BD}) of the gate dielectric.

17. The method of claim 16 wherein the transistor includes a transistor body in the substrate; and comprising coupling the gate dielectric protection module to the transistor body.

18. The method of claim 17 wherein the gate dielectric protection module provides the protection bias to the transistor body to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} to at least 5% below V_{BD}.

~~19. The method of claim 16 wherein the gate dielectric protection module provides the~~ protection bias to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} below V_{BD}.

20. A method for protecting gate dielectric comprising:

providing a transistor at risk;

providing a protection module coupled to the transistor at risk;

activating the protection module to provide a protection bias to reduce a voltage difference between a gate of the transistor at risk and a substrate (V_{DIFF}) to below a breakdown voltage (V_{BD}) of a gate dielectric of the transistor at risk.

CLAIMS

1. A device comprising:

an input/output (I/O) pad; and

an internal circuit, a gate dielectric protection module and an ESD protection circuit, wherein the internal circuit, the gate dielectric protection module and the ESD protection circuit are separate and distinct circuits, and wherein

the internal circuit is coupled between a first power rail which is a high power rail and a second power rail which is a ground rail and the internal circuit is coupled to the I/O pad, the internal circuit comprises a first transistor which is a transistor at risk having a transistor body and a gate, the gate includes a gate electrode over a gate dielectric, wherein the transistor at risk operates normally under normal operational bias voltage when no ESD event and is susceptible to damage and requires protection during an ESD event,

the gate dielectric protection module is coupled to the transistor body of the transistor at risk which functions to protect the gate dielectric of the transistor at risk of the internal circuit during an ESD event, wherein the gate dielectric protection module, when activated, provides a protection bias to the transistor body of the transistor at risk to reduce a voltage difference between the gate of the transistor at risk and substrate (V_{DIFF}) of the transistor at risk to below a breakdown voltage (V_{BD}) of the gate dielectric of the transistor at risk, and

the ESD protection circuit is switched off during no ESD event and provides a current path from the first power rail to the ground rail to dissipate an ESD current during an ESD event.

2. The device of claim 1 wherein the gate dielectric protection module provides the protection bias to the transistor body of the transistor at risk to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} to at least 5% below V_{BD}.

3. The device of claim 1 wherein the gate dielectric protection module provides the protection bias to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} below V_{BD}.

4. The device of claim 1 wherein the gate dielectric protection module provides the protection bias to reduce V_{DIFF} to at least 5% below V_{BD}.

5. The device of claim 1 wherein the gate protection module comprises:

a sensing circuit for detecting an ESD event; and

a biasing circuit coupled to the transistor at risk, wherein

the sensing circuit and biasing circuit are coupled in parallel between the first and second power rails,

the sensing circuit comprises a sensing output which is coupled to a biasing input of the biasing circuit, the sensing circuit activates the biasing circuit when an ESD event is detected to provide the protection bias.

6. The device of claim 5 wherein the sensing circuit comprises:

a sensing resistor coupled in series with a sensing capacitor disposed between the first and second power rails, wherein the sensing resistor is coupled to the first power rail and the sensing capacitor is coupled to the second power rail; and

the sensing circuit output is coupled to the biasing circuit, the sensing circuit output is disposed between a common terminal of the sensing resistor and sensing capacitor,

wherein the sensing circuit generates an inactive sensing output signal at the sensing circuit output when no ESD event is detected and an active sensing output signal when an ESD event is detected to activate the biasing circuit.

7. The device of claim 6 wherein the biasing circuit comprises:

first and second transistors coupled in series between the first and second power rails, a first terminal of the first transistor is coupled to the first power rail and a first terminal of the second transistor is coupled to the second power rail;

the biasing input is coupled to gates of the first and second transistors; and

a biasing output is coupled to common second terminals of the first and second transistors and to the transistor body of the transistor at risk.

8. The device of claim 7 wherein:

the first biasing transistor is a p-type transistor;

the second biasing transistor is a n-type transistor; and

when the protection circuit is activated, the first biasing transistor is switched on and the second biasing transistor is switched off to allow current to flow from the first power rail to the biasing output through the first transistor.

9. The device of claim 8 wherein the current at the biasing output flows to the body of the transistor at risk to produce the protection bias to reduce V_{DIFF}.

10. The device of claim 8 comprises:

a biasing output resistor coupled to the biasing output and the second power rail, wherein the current at the biasing output flows through the resistor to produce the protection bias to reduce V_{DIFF}.

11. The device of claim 5 wherein:

the internal circuit is an inverter which includes an second transistor coupled in series with the transistor at risk between first and second rails, the first terminal of the second transistor is coupled to the first rail and the first terminal of the transistor at risk is coupled to the second rail;

the internal circuit comprises an inverter input which couples the I/O pad to gates of the second transistor and the transistor at risk; and

the internal circuit comprises an inverter output which is coupled to common second terminals of the second transistor and the transistor at risk.

12. The device of claim 11 wherein:

the second transistor is a p-type transistor; and

the transistor at risk is a n-type transistor.

13. The device of claim 5 comprises a rail based ESD protection circuit coupled to the transistor at risk.

14. The device of claim 5 comprises a pad based ESD protection circuit coupled to the transistor at risk.

15. A method for forming a device comprising:

forming an input/output (I/O) pad,

forming an internal circuit, a gate dielectric protection module and an ESD protection circuit, wherein the internal circuit, the gate dielectric protection module and the ESD protection circuit are separate and distinct circuits, and wherein

the internal circuit is coupled between a first power rail which is a high power rail and a second power rail which is a ground rail and the internal circuit is coupled to the I/O pad, wherein forming the internal circuit comprises forming a first transistor which is a transistor at risk having a transistor body and a gate, the gate includes a gate electrode over a gate dielectric, wherein the transistor at risk operates normally under normal operational bias voltage when no ESD event and is susceptible to damage and requires protection during an ESD event, and

the gate dielectric protection module is coupled to the transistor body of the transistor at risk, wherein the gate dielectric protection module functions to protect the gate dielectric of the transistor at risk of the internal circuit during an ESD event and, when activated, provides a protection bias to the transistor body of the transistor at risk to reduce a voltage difference between the gate of the transistor at risk and substrate (V_{DIFF}) of the transistor at risk to below a breakdown voltage (V_{BD}) of the gate dielectric of the transistor at risk, and

the ESD protection circuit is switched off during no ESD event and provides a current path from the first power rail to the ground rail to dissipate an ESD current during an ESD event.

16. The method of claim 15 wherein the gate dielectric protection module provides the protection bias to the transistor body of the transistor at risk to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} to at least 5% below V_{BD}.

17. The method of claim 15 wherein the gate dielectric protection module provides the protection bias to increase the substrate voltage (V_{SUB}) to reduce V_{DIFF} below V_{BD}.

18. A method for protecting gate dielectric comprising:

providing an internal circuit and a protection module, wherein the internal circuit and protection module are separate and distinct circuits and they are not part of an ESD protection circuit, wherein

the internal circuit comprises a first transistor which is a transistor at risk having a transistor body and a gate, the gate includes a gate electrode over a gate dielectric which is to be protected, wherein the transistor at risk operates normally under normal operational bias voltage when no ESD event and is susceptible to damage and requires protection during an ESD event;

the protection module is coupled to the transistor body of the transistor at risk, the protection module functions to protect the transistor at risk of the internal circuit during an ESD event; and

activating the protection module to provide a protection bias to the transistor body of the transistor at risk to reduce a voltage difference between a gate of the transistor at risk and a substrate (V_{DIFF}) of the transistor at risk to below a breakdown voltage (V_{BD}) of a gate dielectric of the transistor at risk, and activating the ESD protection circuit to conduct a current from a first power rail to a ground rail to dissipate an ESD current during an ESD event.

19. The device of claim 1 wherein the ESD protection circuit is coupled to I/O pad and wherein the ESD protection circuit comprises at least one grounded gate n-type MOS

transistor having a drain terminal coupled to the I/O pad and a source terminal and a gate terminal commonly coupled to the ground rail.

20. The device of claim 1 wherein the ESD protection circuit is coupled to the I/O pad and wherein the ESD protection circuit comprises at least one diode pair which is serially coupled between the first and second power rails.