

**STACKED ARRANGEMENT, MICRO-ELECTROMECHANICAL DEVICE AND
METHODS OF FORMING THE SAME**

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of Singapore application No. 10202302727S filed September 26, 2023, the contents of it being hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] Various embodiments of this disclosure may relate to a stacked arrangement. Various embodiments of this disclosure may relate to a method of forming a stacked arrangement. Various embodiments of this disclosure may relate to a micro-electromechanical (MEMS) device. Various embodiments of this disclosure may relate to a method of forming a micro-electromechanical (MEMS) device.

BACKGROUND

[0003] A piezoelectric micro-electromechanical (MEMS) device may include a piezoelectric layer sandwiched between two metal electrodes. Sputter deposition has been widely employed as a deposition method in the manufacturing of good quality piezoelectric MEMS devices. In general, sputter deposited electrodes and piezoelectric layers form fiber-textured films with good out-of-plane orientation, but random in-plane orientation. The lack of in-plane orientation order may result in the film having defects including misoriented grains, high densities of pronounced grain boundaries, dislocations and so forth. For example, piezoelectric scandium aluminum nitride (ScAlN) deposited on a conventional molybdenum (Mo) electrode may exhibit a large number of mis-oriented grains as shown in FIG. 1.

[0004] FIG. 1 shows scanning electron microscopy (SEM) images of misoriented grains in piezoelectric aluminum nitride (AlN) films formed on conventional molybdenum (Mo) electrodes and doped with different concentrations of scandium (Sc). As shown in FIG. 1, the defect density may increase with increasing Sc.

[0005] A high degree of in-plane crystal orientation order in a piezoelectric film can be achieved by forming the device layer stack on a lattice-matched single crystal substrate. However, lattice matched single crystal substrates are rare, expensive, and often not practical for device integration. As the crystallinity of the piezoelectric layer highly depends on the texture and surface morphology of the bottom electrode, improved in-plane orientation order can be achieved by using electrodes which are compliant and highly textured with large grains.

[0006] The approach using a large grain sized bottom electrode to improve in-plane orientation order is a cost-effective solution for reducing defects and getting enhanced performance. However, traditional electrode materials, such as molybdenum (Mo), typically form small grains of size ranging from 20 nm to 40 nm when deposited using standard production tools. In order to form reasonably large Mo grains, a customized deposition tool equipped with very high temperature chucks is required, and that may not be applicable to processes having limited temperature budgets, such as complementary metal oxide semiconductor (CMOS)-MEMS integration. Increasing the electrode thickness may be a way to increase grain size but that may degrade surface roughness and increase parasitic effect. As such, a feasible fabrication method to produce the bottom electrode containing large textured grains at a temperature below 300°C, and yet be within the optimum electrode thickness range may be highly desirable.

SUMMARY

[0007] Various embodiments may relate to a method of forming a stacked arrangement. The stacked arrangement may include a metal electrode layer including a first material. The stacked arrangement may further include a piezoelectric layer. The stacked arrangement may also include a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer. The metal buffer layer may include a second material different from the first material. An average grain size of grains of the metal buffer layer may be greater than an average grain size of grains of the metal electrode layer.

[0008] Various embodiments may relate to a micro-electromechanical systems (MEMS) device. The MEMS device may include a metal electrode layer including a first material. The MEMS device may further include a piezoelectric layer. The MEMS device may also include a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer. The MEMS device may include a further metal electrode layer such that the piezoelectric layer is between the metal electrode layer and the further metal electrode layer. The metal buffer layer may include a second material different from the first material. An average grain size of grains of the metal buffer layer may be greater than an average grain size of grains of the metal electrode layer.

[0009] Various embodiments may relate to a method of forming a stacked arrangement. The method may include forming a metal electrode layer including a first material. The method may also include forming a piezoelectric layer. The method may further include forming a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer. The metal buffer layer may include a second material different from the first material. An average grain

size of grains of the metal buffer layer may be greater than an average grain size of grains of the metal electrode layer.

[0010] Various embodiments may relate to a method of forming a micro-electromechanical systems (MEMS) device. The method may include forming a metal electrode layer including a first material. The method may also include forming a piezoelectric layer. The method may further include forming a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer. The method may additionally include forming a further metal electrode layer such that the piezoelectric layer is between the metal electrode layer and the further metal electrode layer. The metal buffer layer may include a second material different from the first material. An average grain size of grains of the metal buffer layer may be greater than an average grain size of grains of the metal electrode layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily drawn to scale, emphasis instead generally being placed upon illustrating the principles of various embodiments. In the following description, various embodiments of the invention are described with reference to the following drawings.

FIG. 1 shows scanning electron microscopy (SEM) images of misoriented grains in piezoelectric aluminum nitride (AlN) films formed on conventional molybdenum (Mo) electrodes and doped with different concentrations of scandium (Sc).

FIG. 2A is a general illustration of a stacked arrangement according to various embodiments.

FIG. 2B is a general illustration of a micro-electromechanical systems (MEMS) device according to various embodiments.

FIG. 3 is a general illustration of a method of forming stacked arrangement according to various embodiments.

FIG. 4A shows a cross-sectional schematic of the stacked arrangement according to various embodiments.

FIG. 4B shows a top planar view schematic of a piezoelectric layer with long range in-plane order according to various embodiments.

FIG. 4C shows a top planar view schematic of a piezoelectric layer without long range in-plane order.

FIG. 5A is a schematic illustrating the formation of a film over a substrate via deposition according to various embodiments.

FIG. 5B shows a plot of surface energy γ (in Joules per square meter or J/m^2) as a function of various metal surfaces illustrating the surface energies of the various metal surfaces (adopted from theoretical surface energy data) according to various embodiments.

FIG. 6 shows top view scanning electron microscopy (SEM) images ($1\ \mu m \times 1\ \mu m$) of (a) a molybdenum (Mo) metal electrode layer of the stacked arrangement according to various embodiments; (b) a 60 nm aluminum (Al) metal buffer layer formed on the metal electrode layer of the stacked arrangement according to various embodiments; and (c) a 60 nm aluminum (Al) formed directly on a silicon (Si) substrate.

FIG. 7 shows a plot of intensity (in arbitrary units or a.u.) as a function of omega ω (in degrees) illustrating representative rocking curves of aluminum (Al) (111) diffraction peaks of films deposited on different underlayers under different conditions according to various embodiments.

FIG. 8 shows a table illustrating molybdenum (Mo) and aluminum (Al) rocking curve half-maximum (FWHM) data of different stacked arrangements according to various embodiments.

FIG. 9 shows (a) in-plane transmission electron microscopy (TEM) results of the molybdenum (Mo) layer according to various embodiments; (b) ring selected area electron diffraction (SAED) pattern of the molybdenum (Mo) layer according to various embodiments; (c) a plot of count as a function of grain size (in nanometers or nm) illustrating the grain size distribution of the molybdenum (Mo) layer according to various embodiments; (d)) in-plane transmission electron microscopy (TEM) results of the aluminum (Al) layer according to various embodiments; (e) ring selected area electron diffraction (SAED) pattern of the aluminum (Al) layer according to various embodiments; and (f) a plot of count as a function of grain size (in nanometers or nm) illustrating the grain size distribution of the aluminum (Al) layer according to various embodiments.

FIG. 10 shows a table illustrating the scandium aluminum nitride (ScAlN) layer and aluminum (Al) rocking curve half-maximum (FWHM) data of different stacked arrangements according to various embodiments.

FIG. 11A shows (i) a cross-sectional transmission electron microscopy (TEM) image of an scandium aluminum nitride (ScAlN) layer formed on a low temperature (LT) aluminum (Al) layer/ molybdenum (Mo) stack according to various embodiments;; and (ii) a cross-sectional transmission electron microscopy (TEM) image of an scandium aluminum nitride (ScAlN) layer formed on a high temperature (HT) aluminum (Al) layer/ molybdenum (Mo) stack according to various embodiments.

FIG. 11B shows (i) an atomic force microscopy (AFM) image of the scandium aluminum nitride (ScAlN) layer formed on the low temperature (LT) aluminum (Al) layer/ molybdenum (Mo) stack; and (ii) an atomic force microscopy (AFM) image of the scandium aluminum nitride (ScAlN) layer formed on a high temperature (HT) aluminum (Al) layer/ molybdenum (Mo) stack according to various embodiments.

DESCRIPTION

[0012] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0013] Features that are described in the context of an embodiment may correspondingly be applicable to the same or similar features in the other embodiments. Features that are described in the context of an embodiment may correspondingly be applicable to the other embodiments, even if not explicitly described in these other embodiments. Furthermore, additions and/or combinations and/or alternatives as described for a feature in the context of an embodiment may correspondingly be applicable to the same or similar feature in the other embodiments.

[0014] In the context of various embodiments, the articles “a”, “an” and “the” as used with regard to a feature or element include a reference to one or more of the features or elements.

[0015] In the context of various embodiments, the term “about” or “approximately” as applied to a numeric value encompasses the exact value and a reasonable variance, e.g. within 10% of the specified value.

[0016] As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[0017] By “comprising” it is meant including, but not limited to, whatever follows the word “comprising”. Thus, use of the term “comprising” indicates that the listed elements are required or mandatory, but that other elements are optional and may or may not be present.

[0018] By “consisting of” is meant including, and limited to, whatever follows the phrase “consisting of”. Thus, the phrase “consisting of” indicates that the listed elements are required or mandatory, and that no other elements may be present.

[0019] Embodiments described in the context of one of the stacked arrangements/ devices are analogously valid for the other stacked arrangements/ devices, embodiments described in the context of a method are analogously valid for a stacked arrangement/ device, and vice versa.

[0020] Various embodiments may address one or more issues faced by conventional approaches. Various embodiments may be able to create or form long range in-plane order in the piezoelectric layer. Various embodiments may be able to produce or form the bottom electrode containing large textured grains at a temperature below 300°C, with the bottom electrode having a thickness within the optimum electrode thickness.

[0021] FIG. 2A is a general illustration of a stacked arrangement according to various embodiments. The stacked arrangement may include a metal electrode layer 202 including a first material. The stacked arrangement may further include a piezoelectric layer 204. The stacked arrangement may also include a metal buffer layer 206 having a first surface in contact with the metal electrode layer 202 and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer 204. The metal buffer layer 206 may include a second material different from the first material. An average grain size of grains of the metal buffer layer 206 may be greater than an average grain size of grains of the metal electrode layer 202.

[0022] In other words, various embodiments may relate to a stacked arrangement including a metal electrode layer 202, a metal buffer layer 206 on the metal electrode layer 202 and a piezoelectric layer 204 on the metal buffer layer 206. The grain size of the grains contained in the metal buffer layer 206 may be larger than the grain size of the grains contained in the metal electrode layer 202.

[0023] For avoidance of doubt, FIG. 2A seeks to illustrate features of the stacked arrangement, and is not intended to limit, for instance, the dimensions, orientation, shapes etc. of the various features.

[0024] The grain size may refer to a lateral grain size. The lateral grain size of a grain may refer to a diameter or length along a straight line in a lateral plane passing through a center of the grain. The average grain size of a layer may be obtained by summing up all of the grain sizes of the grains contained in the layer, divided by the number of grains contained in the layer. Alternatively, the average grain size of a layer may be obtained by summing up the grain sizes of a sample number of the grains contained in the layer (e.g., across a cross-section), divided by the sample number. The grain size may be measured or determined by microscopy techniques, such as in-plane scanning electron microscopy or other measurement techniques known in the art.

[0025] Due to the larger grain size of the grains in the metal buffer layer 206, the piezoelectric layer 204 in contact with the metal buffer layer 206 may have long range in-plane order. In contrast, for a conventional structure in which the piezoelectric layer is in contact with an electrode with small grain size, the electrode may result in the overlying piezoelectric layer having lack long range in-plane order. A piezoelectric layer with a long range in-plane order may have lower defect density and improved performance as compared to a piezoelectric layer lacking long range in-plane order.

[0026] In various embodiments, the average grain size of the grains of the metal buffer layer 206 may be two times or more than the average grain size of the grains of the metal electrode layer 202.

[0027] In various embodiments, the average grain size of the grains of the metal buffer layer 206 may be greater than 40 nm. In various embodiments, the average grain size of the grains of the metal buffer layer 206 may be greater than 70 nm.

[0028] The larger grain size of the grains in the metal buffer layer 206 relative to those in the metal electrode layer 202 may be due to its lower surface energy. In various embodiments, a surface energy of the metal buffer layer 206 may be lower than a surface energy of the metal electrode layer 202. The surface energy difference between the metal electrode layer 202 and the metal buffer layer 206 may be a key factor leading to the formation of large grains in the metal buffer layer 206, under suitable deposition conditions. A high surface energy difference may be required to achieve lateral growth of grains in the metal buffer layer 206 and to break the grain-to-grain registry between the metal electrode layer 202 and the metal buffer layer 206. The surface energy of a layer may be controlled, for instance, by controlling the material of the layer and/or processing conditions, e.g., temperature.

[0029] For instance, in various embodiments, the metal buffer layer 206 may have a surface energy lower than or equal to 1.5 J/m^2 . In various embodiments, the metal electrode layer 202 may have a surface energy higher than 1.5 J/m^2 .

[0030] In various embodiments, the metal buffer layer 206 may include any suitable material with low surface energy, e.g., surface energy lower than or equal to 1.5 J/m^2 . For instance, the metal buffer layer 206 may include or consist of aluminum (Al), silver (Ag) or zirconium (Zr).

[0031] In various embodiments, the metal electrode layer 202 may include any suitable material with high surface energy, e.g., surface energy higher than 1.5 J/m^2 . For instance, the metal electrode layer 202 may include or consist of molybdenum (Mo), ruthenium (Ru) or tungsten (W).

[0032] In various embodiments, metal electrode layer 202 may be over a substrate. The substrate may be of any suitable material, for instance, silicon, germanium, silicon oxide, sapphire, silicon carbide, or gallium nitride. In various embodiments, the metal electrode layer 202 may be separated from the substrate by a seed layer. The seed layer may be on the substrate, while the metal electrode layer 202 may be on the seed layer. The seed layer may include any

suitable material, such as aluminum nitride (AlN), scandium aluminum nitride (ScAlN), titanium (Ti), tungsten (W) or titanium tungsten (TiW). In various embodiments, the stacked arrangement may include the substrate and/or the seed layer.

[0033] In various embodiments, a thickness of the metal electrode layer 202 may be greater than a thickness of the metal buffer layer 206. The metal electrode layer 202 may form the bulk of the bottom electrode (which may include the metal electrode layer 202, the metal buffer layer 206 and in various embodiments, the seed layer). As the metal buffer layer 206 is configured to result in long-range in-plane order in the piezoelectric layer 206, the metal electrode layer 202 may be free to be configured for optimum performance and integration of the piezoelectric device in which the stacked arrangement may be part of.

[0034] The provision of the metal buffer layer 206 may allow for long range in-plane order of the piezoelectric layer 204 while allowing an overall thickness of the bottom electrode to be kept relatively thin. In various embodiments, an overall thickness of the bottom electrode may, for instance, be equal or less than 400 nm, e.g., equal or less than 300 nm, e.g., equal or less than 300 nm. In various other embodiments, the overall thickness of the bottom electrode may be of any suitable value. The metal buffer layer 206, may for instance, be selected from a range from 10 nm to 80 nm, e.g., from 20 nm to 60 nm. In various other embodiments, the thickness of the metal buffer layer 206 may be of any suitable value. Generally speaking, the texture of the overlying piezoelectric layer 204 may improve as the thickness of the metal buffer layer 206 increases. In various embodiments, a thickness of the metal electrode layer 202 may be selected from a range from 150 nm to 250 nm, e.g., 200 nm. In various other embodiments, the thickness of the metal electrode layer 202 may be of any suitable value. In various embodiments, a thickness of the seed layer may be selected from a range from 10 nm to 60 nm. In various other embodiments, the thickness of the seed layer may be of any suitable value.

[0035] In various embodiments, the piezoelectric layer 204 may include or consist of aluminum nitride (AlN) or a rare earth element doped aluminum nitride. The rare earth element(s) used for doping AlN may, for instance, be or include scandium (Sc) yttrium (Y), lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), promethium (Pm), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb) and/or lutetium (Lu). In various other embodiments, the piezoelectric layer 204 may additionally or alternatively include other piezoelectric material(s), such as zinc oxide (ZnO), lead zirconium titanate (PZT), barium titanate (BaTiO_3), lithium niobate (LiNbO_3), gallium nitride (GaN), and/or indium phosphide (InP).

[0036] FIG. 2B is a general illustration of a micro-electromechanical systems (MEMS) device according to various embodiments. The MEMS device may include the stacked arrangement as shown in FIG. 2A including the metal electrode layer 202, the piezoelectric layer 204 and the metal buffer layer 206. The MEMS device may further include a further metal electrode layer 208 such that the piezoelectric layer 204 is between the metal electrode layer 202 and the further metal electrode layer 208. The dashed lines in FIG. 2B indicate that the further metal electrode layer 208 may, in various embodiments, be separated from the piezoelectric layer 204 by one or more intervening layers, e.g., a diffusion barrier layer, while in various other embodiments, the further metal electrode layer 208 may be in contact with the piezoelectric layer 204.

[0037] For avoidance of doubt, FIG. 2B seeks to illustrate features of the MEMS device, and is not intended to limit, for instance, the dimensions, orientation, shapes etc. of the various features.

[0038] FIG. 3 is a general illustration of a method of forming stacked arrangement according to various embodiments. The method may include, in 302, forming a metal electrode layer

including a first material. The method may also include, in 304, forming a piezoelectric layer. The method may further include, in 306, forming a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer. The metal buffer layer may include a second material different from the first material. An average grain size of grains of the metal buffer layer is greater than an average grain size of grains of the metal electrode layer.

[0039] For avoidance of doubt, FIG. 3 is not intended to limit the sequence of the various steps. In various embodiments, step 302 may occur first, followed by step 306, and then step 304.

[0040] In various embodiments, a seed layer may be formed on a substrate. The metal electrode layer may be formed on the seed layer. The metal buffer layer may be formed on the metal electrode layer. The piezoelectric layer may be formed on the metal buffer layer.

[0041] Various embodiments may be carried out at a temperature below 300 °C. Various embodiments may be CMOS compatible. In particular, the deposition temperature to form the metal buffer layer may be below 300 °C. In various embodiments, the deposition temperature to form the metal buffer layer may be equal or higher than 200 °C (and may be referred to as High Temperature or HT), while in various other embodiments, the deposition temperature to form the metal buffer layer may be equal or lower than 100 °C (and may be referred to as Low Temperature or LT). Generally speaking, the higher the deposition temperature, the greater the grain size of the resultant metal buffer layer.

[0042] In various embodiments, the average grain size of the grains of the metal buffer layer may be two times or more than the average grain size of the grains of the metal electrode layer.

[0043] In various embodiments, the average grain size of the grains of the metal buffer layer may be greater than 40 nm. In various embodiments, the average grain size of the grains of the metal buffer layer may be greater than 70 nm.

[0044] In various embodiments, a surface energy of the metal buffer layer may be lower than a surface energy of the metal electrode layer.

[0045] In various embodiments, the metal buffer layer may have a surface energy lower than or equal to 1.5 J/m^2 .

[0046] In various embodiments, the metal buffer layer may include aluminum (Al), silver (Ag) or zirconium (Zr).

[0047] In various embodiments, the metal electrode may include molybdenum (Mo), ruthenium (Ru) or tungsten (W).

[0048] In various embodiments, the piezoelectric layer may include aluminum nitride (AlN) or a rare earth element doped aluminum nitride.

[0049] Various embodiments may relate to a method of forming a micro-electromechanical systems (MEMS) device. The method of forming the MEMS device may include steps 302, 304, and 306 as illustrated in FIG. 3, and may further include forming a further metal electrode layer such that the piezoelectric layer is between the metal electrode layer and the further metal electrode layer. In various embodiments, the further metal electrode layer may be formed after forming the piezoelectric layer.

[0050] Various embodiments may relate to an efficient and manufacturable method to form a high quality pseudo-epitaxial AlN or ScAlN film with long range in-plane orientation order. Various embodiments may relate to forming a highly textured electrode layer (i.e., metal buffer layer), whereby accelerated lateral grain growth may be achieved by both material selection and deposition conditions optimization.

[0051] In various embodiments, the stacked arrangement may be a multi-layer structure including a textured first metal layer (i.e., metal electrode layer) disposed on a seed layer, and a second metal layer (i.e., metal buffer layer) disposed on the first metal layer. The second metal layer may be highly textured with lateral grain size substantially larger than the grains in the

first metal layer. The first metal layer may form the bulk of the bottom electrode and may be configured for optimum performance and integration of device.

[0052] FIG. 4A shows a cross-sectional schematic of the stacked arrangement according to various embodiments. The stacked arrangement may include a substrate 408, a seed layer 410 on the substrate 408, a first metal layer 402 (alternatively referred to as metal electrode layer) on the seed layer 410, a second metal layer 406 (alternatively referred to as a metal buffer layer) on the first metal layer 402, and a piezoelectric layer (e.g., AlN or ScAlN) layer 404 on the second metal layer 406.

[0053] The first metal layer 402 may have smaller grain size. The larger grains in the second metal layer 406 may result in long range in-plane order in the overlying piezoelectric layer 404. FIG. 4B shows a top planar view schematic of a piezoelectric layer with long range in-plane order according to various embodiments. FIG. 4C shows a top planar view schematic of a piezoelectric layer without long range in-plane order. The ordered group of grains may act as a large single grain, like a pseudo-epitaxy layer. This may effectively reduce grain boundary thickness and may eliminate or reduce grain boundary effects.

[0054] Attempts to integrate a multi-layered electrode to the MEMS structures for improving texture, reducing electrical loss, and altering polarity have been reported earlier. Various embodiments as described herein may relate to a stacked arrangement including a second metal layer 406 (i.e., metal buffer layer) with enlarged grain size to achieve pseudo-epitaxial AlN/ScAlN with large range in-plane orientation order, as well as the corresponding method of fabrication.

[0055] The first metal layer 402 may include a metal which is traditionally used for electrodes in piezoelectric MEMS devices. High acoustic impedance metals such as Mo, Ru and W may be suitable choices as the material for first metal layer 402. Interestingly, all these metals exhibit a high surface energy. Subsequently, a second metal layer 406 with substantially

lower surface energy may be deposited on the first metal layer 402. Due to a large difference in surface energies, the deposition to form the second metal layer 406 may tend to follow an accelerated lateral growth mode to cover the surface of high surface energy first metal layer 402. Such growth may result in large grains or crystals if process conditions are chosen appropriately.

[0056] FIG. 5A is a schematic illustrating the formation of a film over a substrate via deposition according to various embodiments. In the initial stage of deposition (denoted as (a) in FIG. 5A), the deposited adatoms may form islands. As more adatoms are deposited, the islands may coalesce to form a smooth film, as shown in (b). Subsequently, as more atoms are deposited, islands may be formed over the smooth film, as shown in (c). When a material with lower surface energy is deposited on an underlying layer with more surface energy, the atoms of the lower surface energy may tend to spread out more over the underlying layer and coalesce to form a smooth film with large grains (instead of forming islands to form a rough film with small grains).

[0057] FIG. 5B shows a plot of surface energy γ (in Joules per square meter or J/m^2) as a function of various metal surfaces illustrating the surface energies of the various metal surfaces (adopted from theoretical surface energy data) according to various embodiments. It may be seen that the surface energy of Al may be less than half of that of Mo.

[0058] It may be seen from FIG. 5B that metals such as Al, Ag and Zr show much lower surface energies compared to Mo, Ru & W, and may be used as the material for the second metal layer 406 from the surface energy viewpoint. As both Al and Ag metals are malleable and provide hexagonal arrangement of atoms when deposited over Mo, W or Ru, they may be suitable as candidate materials for the second metal layer 406. Being malleable may provide compliant seeding (adjusting lattice with Sc concentration in piezoelectric layer 404) and the

hexagonal arrangement may keep the lattice strain to minimum, as AlN and ScAlN also form hexagonal arrangement of atoms.

[0059] In order to demonstrate this hypothesis, a stacked arrangement with a first metal layer including Mo and a second metal layer including Al was fabricated. The deposition conditions for forming the second metal layer may be adjusted or optimized to obtain the desired properties. Subsequently, ScAlN with a desired Sc percentage may be deposited to form the piezoelectric layer. Characterization may be carried out to assess the quality of the as-deposited stacked arrangement.

[0060] FIG. 6 shows top view scanning electron microscopy (SEM) images ($1\ \mu\text{m} \times 1\ \mu\text{m}$) of (a) a molybdenum (Mo) metal electrode layer of the stacked arrangement according to various embodiments; (b) a 60 nm aluminum (Al) metal buffer layer formed on the metal electrode layer of the stacked arrangement according to various embodiments; and (c) a 60 nm aluminum (Al) formed directly on a silicon (Si) substrate. The atomic force microscopy (AFM) roughness (Ra) values are indicated on the respective images. The aluminum (Al) is deposited at temperatures $\leq 100\ ^\circ\text{C}$. It can be seen from FIG. 6(a) that Mo film deposited on AlN seed layer exhibits granular surface morphology with roughness (Ra) of about 0.7 nm. On the other hand, as shown in FIG. 6(b), the Al layer deposited at $\leq 100^\circ\text{C}$ (not fully optimized) on Mo layer renders a smooth surface morphology. A significant reduction in surface roughness was observed with Ra reduced to about 0.4 nm after 60 nm Al deposition on the Mo bottom layer. As a comparison, Al film of 60 nm was deposited on Si substrate under similar deposition conditions and characterized. FIG. 6(c) shows a distinct surface morphology with Ra of about 4.3 nm for Al film deposited directly on silicon substrate. Similar rough film morphology and presence of hillocks may be inherent to Al films and were reported elsewhere.

[0061] The texture properties of the deposited films were characterized by recording X-ray diffraction (XRD) ω -scan (rocking curve). FIG. 7 shows a plot of intensity (in arbitrary units

or a.u.) as a function of omega ω (in degrees) illustrating representative rocking curves of aluminum (Al) (111) diffraction peaks of films deposited on different underlayers under different conditions according to various embodiments. High Temperature (HT) refers to deposition at a high temperature of $\geq 200^{\circ}\text{C}$, while Low Temperature (LT) refers to deposition at a lower temperature of $\leq 100^{\circ}\text{C}$. The Al film on Mo curves show narrower rocking curves with smaller full-width at half-maximum (FWHM) suggesting good texture compared to the curve of Al film deposited directly on Si substrate. Further efforts were made to improve Al (111) texture as it may be a critical parameter determining c-axis orientation in the subsequently deposited AlN or ScAlN functional layer. Amongst various parameters, providing high substrate temperature may be found to be effective in obtaining a highly textured Al film on Mo. A FWHM of 0.7° for 60 nm Al film on Mo may be achieved by using a substrate temperature of about 250°C and adjusting deposition parameters. This is best reported FWHM value for such a thin Al layer.

[0062] Next, Al films were deposited on other potential underlayers such as AlN to understand the effect of underlayers on texture and film growth behavior. In addition, thinner Al layers were also deposited and characterized for minimum loading effects. FIG. 8 shows a table illustrating molybdenum (Mo) and aluminum (Al) rocking curve half-maximum (FWHM) data of different stacked arrangements according to various embodiments. Evidently, the Al film deposited on textured Mo (110) films at a relatively high temperature may exhibit strong (111) texture (low FWHM values).

[0063] The grain size of the first metal layer (Mo) and second metal layer (Al) were analysed using in-plane transmission electron microscopy (TEM) results inspection. FIG. 9 shows (a) in-plane transmission electron microscopy (TEM) results of the molybdenum (Mo) layer according to various embodiments; (b) ring selected area electron diffraction (SAED) pattern of the molybdenum (Mo) layer according to various embodiments; (c) a plot of count as a

function of grain size (in nanometers or nm) illustrating the grain size distribution of the molybdenum (Mo) layer according to various embodiments; (d)) in-plane transmission electron microscopy (TEM) results of the aluminum (Al) layer according to various embodiments; (e) ring selected area electron diffraction (SAED) pattern of the aluminum (Al) layer according to various embodiments; and (f) a plot of count as a function of grain size (in nanometers or nm) illustrating the grain size distribution of the aluminum (Al) layer according to various embodiments.

[0064] As shown in FIG. 9(b), the Mo layer deposited using baseline recipe shows grains with random orientation as revealed from the ring selected area electron diffraction (SAED) pattern (zone axis along the film normal). As illustrated by FIG. 9(c), the Mo grain sizes may range from about 10 nm to about 40 nm, and the average grain size was found to be about 20.8 nm. The SAED and in-plane-inspection on the Al layer also revealed a granular microstructure. However, the in-plane grain size was substantially larger compared to that of the Mo layer. The average in-plane grain size of Al layer was about 74.1 nm. Remarkably, several large grains with sizes well above 100 nm were observed in the Al layer.

[0065] The formation of large lateral sized and highly textured Al grains on Mo may be due to the combined effects of energetic and kinetic factors. At the initial nucleation and growth stage, Al grains laterally grow to reduce total energy. The high mobility deposition conditions including high temperature favor the formation of large lateral sized grains in thinner films. The high mobility of Al adatoms on Mo surface may also likely favor the formation of large grains.

[0066] The benefit of multiple layers in the bottom electrode was evaluated by depositing and characterizing the ScAlN layer. A Sc-Al alloy target with Sc content of 30 atomic percentage was selected for the formation of ScAlN film via reactive sputtering. All the layers including the AlN seed layer, the first metal layer (Mo), the second metal layer (Al) and the ScAlN layer were deposited without breaking the vacuum in a cluster deposition tool with

multiple single target chambers. A previously established process of record ScAlN deposition conditions was employed for the fabrication of the test stacked arrangements to characterize the performance of various bottom electrodes. The insertion of the second metal layer was found to significantly reduce the abnormal grains in the ScAlN layer. The thickness of the second metal layer (Al) was varied to optimize the ScAlN film properties. The XRD rocking curve FWHM of Al and ScAlN layers of various stacked arrangements with varying Al layer thicknesses is summarized in FIG. 10. FIG. 10 shows a table illustrating the scandium aluminum nitride (ScAlN) layer and aluminum (Al) rocking curve half-maximum (FWHM) data of different stacked arrangements according to various embodiments. FIG. 10 shows that the texture of the ScAlN layer may improve with the thickness of the Al layer. The improvement in ScAlN texture may be likely due to a combined effect of Al material properties and its texture.

[0067] The microstructure of the stacked arrangement may be further characterized using cross-sectional TEM. FIG. 11A shows (i) a cross-sectional transmission electron microscopy (TEM) image of an scandium aluminum nitride (ScAlN) layer formed on a low temperature (LT) aluminum (Al) layer/ molybdenum (Mo) stack according to various embodiments; and (ii) a cross-sectional transmission electron microscopy (TEM) image of an scandium aluminum nitride (ScAlN) layer formed on a high temperature (HT) aluminum (Al) layer/ molybdenum (Mo) stack according to various embodiments. FIG. 11B shows (i) an atomic force microscopy (AFM) image of the scandium aluminum nitride (ScAlN) layer formed on the low temperature (LT) aluminum (Al) layer/ molybdenum (Mo) stack; and (ii) an atomic force microscopy (AFM) image of the scandium aluminum nitride (ScAlN) layer formed on a high temperature (HT) aluminum (Al) layer/ molybdenum (Mo) stack according to various embodiments.

[0068] Piezoelectric coefficients of the ScAlN may be obtained from the double beam laser interference (DBLI) method to confirm the film quality. As compared to the average $d_{33,f}$ value

10.6 pm/V of the piezoelectric layer corresponding to the Al metal buffer layer formed under a low temperature (FIG. 11A (i)), the piezoelectric layer corresponding to the Al metal buffer layer formed under a high temperature may show an average $d_{33,f}$ value of 11.0 pm/V (FIG. 11A (ii)), indicating a substantial improvement in the piezoelectric properties. The improved piezoelectric properties of ScAlN films in the stacked arrangement according to various embodiments can be attributed to several factors including reduced defects and improvements in texture of the ScAlN films.

[0069] Various embodiments may relate to a multilayer electrode structure including a relatively thicker first metal layer, and a thin second metal layer on the first metal layer, wherein the second metal layer forms highly textured large sized lateral grains compared to the first metal layer. Various embodiments may relate to a method to form such multi-layered electrode structure via material selection (based on surface energy) and/or deposition condition optimization. The ScAlN film deposited on the electrode with the metal buffer layer may possess a long range in-plane orientation order and may demonstrate enhanced piezoelectric properties.

Claims

1. A stacked arrangement comprising:
 - a metal electrode layer comprising a first material;
 - a piezoelectric layer; and
 - a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer;wherein the metal buffer layer comprises a second material different from the first material; and
wherein an average grain size of grains of the metal buffer layer is greater than an average grain size of grains of the metal electrode layer.
2. The stacked arrangement according to claim 1,
 - wherein the average grain size of the grains of the metal buffer layer is two times or more than the average grain size of the grains of the metal electrode layer.
3. The stacked arrangement according to claim 1,
 - wherein the average grain size of the grains of the metal buffer layer is greater than 40 nm.
4. The stacked arrangement according to claim 1,
 - wherein the average grain size of the grains of the metal buffer layer is greater than 70 nm.

5. The stacked arrangement according to claim 1,
wherein a surface energy of the metal buffer layer is lower than a surface energy of the metal electrode layer.
6. The stacked arrangement according to claim 1,
wherein the metal buffer layer has a surface energy lower than or equal to 1.5 J/m².
7. The stacked arrangement according to claim 1,
wherein the metal buffer layer comprises aluminum (Al), silver (Ag) or zirconium (Zr).
8. The stacked arrangement according to claim 1,
wherein the metal electrode layer comprises molybdenum (Mo), ruthenium (Ru) or tungsten (W).
9. The stacked arrangement according to claim 1,
wherein the piezoelectric layer comprises aluminum nitride or a rare earth element doped aluminum nitride.
10. A micro-electromechanical systems (MEMS) device comprising:
a metal electrode layer comprising a first material;
a piezoelectric layer;
a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer; and

a further metal electrode layer such that the piezoelectric layer is between the metal electrode layer and the further metal electrode layer;
wherein the metal buffer layer comprises a second material different from the first material; and
wherein an average grain size of grains of the metal buffer layer is greater than an average grain size of grains of the metal electrode layer.

11. A method of forming a stacked arrangement, the method comprising:
forming a metal electrode layer comprising a first material;
forming a piezoelectric layer; and
forming a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer;
wherein the metal buffer layer comprises a second material different from the first material; and
wherein an average grain size of grains of the metal buffer layer is greater than an average grain size of grains of the metal electrode layer.
12. The method according to claim 11,
wherein the average grain size of the grains of the metal buffer layer is two times or more than the average grain size of the grains of the metal electrode layer.
13. The stacked arrangement according to claim 11,
wherein the average grain size of the grains of the metal buffer layer is greater than 40 nm.

14. The stacked arrangement according to claim 11,
wherein the average grain size of the grains of the metal buffer layer is greater than 70 nm.
15. The stacked arrangement according to claim 11,
wherein a surface energy of the metal buffer layer is lower than a surface energy of the metal electrode layer.
16. The stacked arrangement according to claim 11,
wherein the metal buffer layer has a surface energy lower than or equal to 1.5 J/m².
17. The stacked arrangement according to claim 11,
wherein the metal buffer layer comprises aluminum (Al), silver (Ag) or zirconium (Zr).
18. The stacked arrangement according to claim 11,
wherein the metal electrode layer comprises molybdenum (Mo), ruthenium (Ru) or tungsten (W).
19. The stacked arrangement according to claim 11,
wherein the piezoelectric layer comprises aluminum nitride or a rare earth element doped aluminum nitride.
20. A method of forming a micro-electromechanical systems (MEMS) device, the method comprising:
forming a metal electrode layer comprising a first material;

forming a piezoelectric layer;

forming a metal buffer layer having a first surface in contact with the metal electrode layer and a second surface, the second surface opposite the first surface, in contact with the piezoelectric layer; and

forming a further metal electrode layer such that the piezoelectric layer is between the metal electrode layer and the further metal electrode layer;

wherein the metal buffer layer comprises a second material different from the first material; and

wherein an average grain size of grains of the metal buffer layer is greater than an average grain size of grains of the metal electrode layer.