

Specification

The invention relates to a system for the digital transmission of information, particularly for digital transmission via satellites, in accordance with the preamble to Claim 1.

In bit-serial data transmission, the data blocks consisting of code words, namely frames and possibly sub-frames, are repeated periodically. In order to be able to decode the data blocks correctly, it is necessary to know the position of the frame in time. When self-synchronizing codes are used, the bandwidth of the transmission is increased by increased redundancy requirements. A so-called decimal-point code avoids an appreciable increase in the bandwidth. Particularly with 4-phase CPSK modulation, the data regeneration is ensured by a decimal-point code based on the frame structure. CPSK stands for coherent phase shift keying.

In this case, each transmission block of the digital signal contains a preceding code word, the synchronization word, which serves to identify the synchronization. This is generally followed by a sequence of data code words which also contain checking information.

Time errors and amplitude errors may occur in the transmission path to be considered. During the timing regeneration, time errors cause so-called bit slips. Amplitude errors, that is to say bit inversions, distort data and synchronization word. When a 4-phase CPSK modulation is used, it is necessary to compensate the ambiguity of the phase demodulation during the data regeneration. Synchronization words are known from the literature (Barker, Maury) wherein a small number of bit errors in a synchronization word do not impair the definite identification of the synchronization word.

A digital signal transmission system is known from DE-A 1 30 13 554 wherein synchronization words are transmitted and processed serially in a single data stream.

In this case, two comparators are used which do not work simultaneously and which examine the data stream for the different synchronization words. It is not possible to eliminate phase ambiguity by the above method.

It is the object of the invention to improve the recognition of the position in time of the data stream in a system for the digital transmission of information signals, and to compensate the influence of time errors, amplitude errors and phase ambiguities.

The problem is solved by the invention given in Claim 1. Further developments of the invention are described in sub-claims.

By using the system according to the invention, the position in time of the frame is recognized with sufficient certainty. The length of the synchronization word is relatively short in relation to the subframe length and the associated redundancy is minimal. The synchronization words are selected so that a failure of the synchronization occurs considerably more rarely than errors which cannot be corrected in the information.

For the recognition of the synchronization words at the receiving end, the words have to be considered in an excellent position in time in correlators. In the undisplaced position of the autocorrelation function, that is to say for the moment $T = 0$, the synchronization words contain a pronounced maximum. For all moments $T \neq 0$, the autocorrelation function is minimal in amount.

A CPSK modulation has a phase ambiguity. This can lead to the fact that the synchronization word arrives at the receiver in an inverted position. The synchronization words therefore comprise a very small difference between autocorrelation function and inverted autocorrelation function for all moments $T \neq 0$, so that the synchronization words are reliably recognized even in the inverted position.

The ambiguity in the CPSK demodulation can be compensated by the evaluation of the correlation function formed in

the receiver between the stored sync word and the received sync word. The position in time of the beginning of the frame is determined by the result of the value determined in the correlator and by a following threshold logic in so far as the control signals derived from both correlators are supplied to a logic circuit, which are interrogated in a defined data window.

For the correction of time errors which may lead to a bit slip, it is proposed to check the cross correlation function in a slightly widened data window. With reference to the position of the maximum of the cross correlation function within this data window, a direct conclusion can be drawn about the occurrence and magnitude of a bit slip and be corrected for the next frame. For this purpose, the cross correlation function for the moment $T = 0$ must be greater in amount than the cross correlation function for moments $T \neq 0$. This is only possible, however, up to a maximum number of bit errors in the synchronization word. The maximum permissible number of bit errors is the greater, the longer the synchronization word is selected. A favourable compromise was reached between the two requirements of small redundancy and high probability of residual errors.

As a result of the synchronization words, with a length of the synchronization word of 16 bits, up to any 3 bit errors can be permitted in a synchronization word without the unambiguity of the recognition of the synchronization word being lost. If the width of the window for checking the synchronization word is more than 1 bit, it must be borne in mind that the synchronization word may be distorted by bit errors caused by the disturbed channel and by neighbouring data.

With a window width of five timing pulses, bit slips of up to ± 2 timing pulses can be detected through the synchronization words by means of a threshold logic and the shift in time can be eliminated. In order to meet the criterion that the failure of the synchronization should

occur considerably more rarely than is presupposed by the maximum permissible residual error probability for distorted information which cannot be corrected, it is proposed, with a division of the main frame into two subframes (digit planes A and B), to provide the same or an equivalent pattern of the same length for the synchronization in both subframes. With a correlator for each of the subframes A and B, the two synchronization words can be checked simultaneously, the position in time of the frame can be recognized therefrom and the ambiguity in the phase demodulation can be eliminated. As a result of the use of this system for the frame synchronization, synchronization errors only occur if both synchronization words are each disturbed by four bit errors.

The invention is described in more detail below with reference to an example of embodiment.

Figure 1 shows a block circuit diagram for the evaluation of the synchronization words in the subframes A and B,

Figure 2 shows a block circuit diagram for determining the cross correlation function,

Figure 3 shows a forked circuit,

Figure 4 shows a table,

Figure 5 shows a circuit for determining the position of the synchronization word,

Figure 6 shows an operation control.

Figure 1 shows a block circuit diagram for the recognition of the synchronization words. The signal arriving at the terminal 1 is fed to a 4-phase demodulator 2 (CSPK). The data stream is divided into two digit planes A and B. Since the demodulation in the CPSK demodulator 2 is ambiguous, the signals A, B may appear inverted or non-inverted, that is to say there are two possibilities for each digit plane. The data of each digit plane are supplied to shift registers 3 and 4 respectively. The cross correlation function is formed in the stage 5 or 6

respectively by comparison of the data read into the shift registers 3, 4 with the synchronization word wired-in by a circuit arrangement 44, Figure 2. The stages 5 and 6 are each storage modules which are divided into two parts. By addition of the contents of the called-up addresses of the stores in the addition stages 7 and 8 respectively, the particular value of the cross correlation function can be determined. A following threshold logic 9 or 10 respectively distinguishes, with reference to the input cross correlation value, between whether the sync word or its inversion or no sync word has been received. In the stage 11, the position in time of the synchronization word is established and the internal frame timing is possibly re-adjusted. It can likewise be ascertained whether the component data streams A and B have been received in the inverted, non-inverted and/or interchanged position. If necessary, the component data streams are corrected by means of the forked circuit 12.

Figure 2 shows a circuit diagram for determining the cross correlation function. The data stream passes from the terminal 13 serially into the shift register 3. A bit sequence of 16 bits appears at each of the parallel outputs of the shift register 3. 8 bits of each of the data words appearing at the parallel outputs of the shift register 3 are compared with the corresponding component code word of the synchronization word through exclusive OR gates 47-49 and 50-52 respectively. The outputs of the exclusive OR gates are fed to a Prom (PROM = programmable read only memory) 14 or 15 respectively. The particular data pattern appearing at the eight outputs of the exclusive OR gates 47-49 and 50-52 respectively indicates an address in the prom circuits 14 or 15. The contents of the called-up store locations of the prom circuits 14 and 15 are fed to an adder 7. Depending on the code word which appears at the outputs of the shift register 3, certain addresses are called up in each of the PROM circuits 14 and 15,

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which addresses call up a store content between -4 and +4 in binary coded form which corresponds to the particular number of agreements. The addition in the adder 7 gives the value of the cross correlation function (-8 to +8). The two most significant bits of the store contents appearing at the outputs of the PROM circuits 14 and 15 are fed to an exclusive OR gate 16. The output of the exclusive OR gate 16 and the most significant digit of the output of the adder 7 pass to a further exclusive OR gate 17, the output of which represents the most significant bit of the cross correlation value appearing at the output of the adder 7, in the two's complement. The output of the adder 7, together with the output of the exclusive OR gate 17, represents the determined value of the cross correlation function which is represented in the two's complement.

At the same time, the output signal of the exclusive OR gate 17 is the most significant bit and thus represents the sign of the cross correlation function.

A further PROM circuit 18 is controlled by the values at the output of the adder 7 and at the output of the exclusive OR gate 17.

If the address code words applied to the PROM circuit 18 exceed a preset threshold in the value of their significance, the associated store locations are distinguished by a logical "1". A called-up store content of logical "1" which is given out at terminal 19 indicates the recognition of a synchronization word while the state of the terminal 22 indicates whether there is an inverted or non-inverted position.

Figure 3 shows a forked circuit which is controlled by the signals E and F at the terminals 22 and 23.

The signals E and F come from the correlators for the digit planes A and B and correspond to the particular most significant bit of the correlator output signal of A and B. The circuit shown in Figure 3 is built up on the following structure:

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$$C = (E.F + \bar{E}.F) \cdot (A.E + \bar{A}.E) + (E.F + F.E) \cdot (B.F + \bar{B}.F)$$

$$D = (E.F + \bar{E}.F) \cdot (B.F + \bar{B}.F) + (E.F + F.E) \cdot (A.E + \bar{A}.E)$$

The output signals C and D at terminals 24 and 25 of the forked circuit of Figure 3 result with an input signal A and B at terminals 20 and 21, depending on the control information at terminals 22 and 23. By means of this circuit, two data streams can either be exchanged or/and inverted (see Figure 4).

Figure 5 shows a circuit for recognizing the position of the synchronization pattern in the frame. The signals of the store locations of a PROM circuit 18, as illustrated in Figure 2, are fed to the terminals 19 and 27. A shift register 28 or 29 is provided for each subframe. The shift registers 28 and 29 each contain 5 bit cells to the middle values of which there is connected an AND gate 30. Furthermore, there are strobe inputs 31 and 32 respectively. The parallel outputs of the shift registers 28 and 29 lead to a 1024 x 4 PROM circuit 33. The contents of the addressed store locations of the PROM circuit 33 pass to an adder 34 to which counter contents from a preprogrammable frame counter 26, 36 are likewise fed. In the example illustrated, the counter counts up to an address 320 each time. As soon as the counter has reached its end address, a pulse is fed to its load input 37 and the counter is again reset to the preprogrammable initial state.

In order to search for the frame timing for the first time, a signal is fed to the restart input 39 and sets the counter 36 afresh. At the same time, the strobe inputs 31 and 32 of the shift registers 28 and 29 are actuated through the OR gate 40. Since the outputs of the shift registers 28 and 29 lead to the PROM circuit 33, a specific address of the PROM circuit 33 is addressed each time. The outputs of the correlator threshold logic of the digit planes A and B are connected to the serial inputs of the shift registers 19 and 27 through the terminals 19 and 27.

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The position of the data window obtained from the operation control is present at terminal 38. It is applied to the strobe inputs 31 and 32 via the STROBE gate 40.

The information read into the shift registers 28 and 29 after 5 timing pulses appearing in the data window is then evaluated by means of the contents of the PROM circuit 33. The contents of the store location of the called-up address gives the adder 34 the information as to how far away the present timing pulse is from the frame timing pulse. In the desired position of the synchronization timing pulse, the timing pulse is in the middle storage cells of the shift registers 28 and 29. Through the AND gate 30 connected thereto, a pulse is delivered to the terminal 41. Through an evaluation logic which is connected up and which is illustrated in Figure 6, a pulse is delivered to the load input 37 via the terminal 39. Thereupon, the counter 36 begins to count afresh. If the desired position is not reached, for example as a result of a bit slip, the counting total of the counter 36 is altered through another called-up address of the PROM circuit 33. Thereupon, the timing-pulse synchronization of the frame is displaced in the correct manner.

Figure 6 shows an evaluation logic to control the course of the search and hold operation. The position information of the synchronization word from the two sub-frames A, B is fed to the terminals 22 and 23. As soon as the synchronization word is present in the correct position in time, the input terminal 41 receives a pulse from the AND gate 30. The search mode is initiated by a change of state to logical 1 at the terminal 38 which leads to the OR gate 40. A pulse at the terminal 39 passes via an OR gate to the load input 37 of the counter 36 and causes a fresh start of the frame counter 36. The signal at the load input 37 represents the frame timing pulse at the same time.

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The PROM circuit 33 only delivers a pulse to the terminal 43 if no synchronization word is found. The pulse at the terminal 43 passes to an OR gate 45 to the terminal 46 of which there can be applied a pulse for initializing the whole circuit for the first time. The PROM circuits 18 of the circuit shown in Figure 2 for the two subframes are connected to the terminal 42 so that the threshold values for the cross correlation function fixed by means of the PROM circuits 18 can be changed over.

Claims

1. A system for the transmission and reception of digital information signals, particularly for digital sound transmission via satellites wherein the data sequences are arranged following one another in time in a frame, and wherein, in the receiver, the frame is divided into subframes (A, B) which are parallel in time and represent the data sequences, characterised in that each subframe (A, B) comprises a synchronization word of the same or equivalent type of the same length, that a correlator (3, 5, 7; 4, 6, 8; 3, 7, 14, 15, 44, 47-52) is used for each subframe (A, B) for the time recognition and if necessary to compensate for the phase position of the subframes (A, B), that code words which have an unequivocal maximum of their autocorrelation function for the moment $T = 0$ are used for the synchronization and that the autocorrelation function is minimum for all moments $T \neq 0$.

2. A system according to Claim 1, characterised in that one of the following synchronization words, their inversion, mirror image (read backwards) or inverted mirror image is used, 0 representing logical 0 and 1 representing logical 1:

1. 0110100001110111
2. 0101101110111000
3. 0100100010001111
4. 0100010010111100

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3. A system according to Claim 1, characterised in that a circuit arrangement (Figure 5) is present for recognizing the position in time of the synchronization word and for correcting the position in time of the frame.

4. A system according to Claim 1, characterised in that a circuit (Figure 3) for exchanging the incoming data streams (A and B) is provided which is controlled by a synchronization-word recognition circuit.

5. A system according to Claim 1, characterised in that in order to find out the synchronization state for the first time or again, the presence of the synchronization word is checked twice.

6. A system according to Claim 1, characterised in that two operating states are provided and in a first operating state, the presence of the synchronization pattern is checked twice and if the synchronization pattern is recognized, switching over into the second operating state is effected in which the phase position of the data sequence is checked for ± 2 bit timing pulses from the normal state and in the event of deviation from the normal state a time correction is effected immediately in the next frame.

7. A system according to Claim 1, characterised in that in order to determine the synchronization word, two storage modules (14, 15) are used, the outputs of which give the value of the cross correlation between the stipulated and the received synchronization word, via an addition circuit (7).

8. A circuit according to Claim 1, characterised in that a threshold logic is present which contains a storage module (18) in which an address, under which the representative values for the states: sync word present, inverted sync word present and no sync word present, are stored, is associated with each cross correlation value.



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Figure 1

Sync. (yes/no)
Frame sequence

Figure 2

Hold mode

Figure 5

Search mode

Data window signal

PROM

Load Counter
Preprogramming

Figure 6

Frame timing pulses

Preparatory flip-flop

Mode flip-flop

Search mode
Frame restart

