INTEGRATED CIRCUIT PACKAGE AND FLAT PLATE MOLDING PROCESS FOR INTEGRATED CIRCUIT PACKAGE

ABSTRACT OF THE DISCLOSURE

An integrated circuit package having a top opening and a cavity, with a chip adhered in the cavity. The top opening has routing strips electrically connecting the top opening with the outer surface. The routing strips are electronically connected to bonding pads located in a central area of the chip. Following assembly of the components, the top opening and the cavity are encapsulated in a molding process. A method is provided for forming a substantially flat integrated circuit package.

Figure 1

This Sheet Has Been Replaced

