

ABSTRACT

A memory device comprises a memory cell array including first and second planes; a page buffer circuit including first cache latches for storing data to be stored in the first plane and second cache latches for storing data to be stored in the second plane; and input/output lines for receiving a command and addresses from a memory controller. The command includes target plane information for initializing the first cache latches and/or the second cache latches. The memory device initializes only cache latches of a target plane according to the command including the target plane information.

FIG.8