PITCH MULTIPLICATION SPACERS AND METHODS OF FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to the following: U.S. Patent Application No. 10/934,778 to Abatchev *et al.*, filed September 2, 2004, entitled Method for Integrated Circuit Fabrication Using Pitch Multiplication; and U.S. Patent Provisional Application No. 60/662,323 to Tran *et al.*, filed March 15, 2005, entitled Pitch Reduced Patterns Relative To Photolithography Features.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates generally to integrated circuit fabrication and, more particularly, to masking techniques.

Description of the Related Art

[0003] As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency, integrated circuits are continuously being made more dense. The sizes of the constituent features that form the integrated circuits, *e.g.*, electrical devices and interconnect lines, are constantly being decreased to facilitate this scaling.

[0004] The trend of decreasing feature size is evident, for example, in memory circuits or devices such as dynamic random access memories (DRAMs), flash memory, static random access memories (SRAMs), ferroelectric (FE) memories, etc. These memory devices typically comprise millions of identical circuit elements, known as memory cells. A capacitor-based memory cell, such as in conventional DRAM, typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that can store one bit (binary digit) of data. A bit can be written to a cell through the transistor and can be read by sensing charge in the capacitor. Some memory technologies employ elements that can act as both a storage device and a switch (*e.g.*, dendritic memory employing silver-doped chalcogenide glass)

and some nonvolatile memories do not require switches for each cell (*e.g.*, magnetoresistive RAM). In general, by decreasing the sizes of the electrical devices that constitute a memory cell and the sizes of the conducting lines that access the memory cells, the memory devices can be made smaller. Additionally, storage capacities can be increased by fitting more memory cells on a given area in the memory devices.

[0005] The continual reduction in feature sizes places ever greater demands on the techniques used to form the features. For example, photolithography is commonly used to pattern features, such as conductive lines. The concept of pitch can be used to describe the sizes of these features when the pattern includes repeating features, as in arrays. Pitch is defined as the distance between an identical point in two neighboring features. These features are typically defined by spaces between adjacent features, which spaces are typically filled by a material, such as an insulator. As a result, pitch can be viewed as the sum of the width of a feature and of the width of the space on one side of the feature separating that feature from a neighboring feature. However, due to factors such as optics and light or radiation wavelength, photolithography techniques each have a minimum pitch below which a particular photolithographic technique cannot reliably form features. Thus, the minimum pitch of a photolithographic technique is an obstacle to continued feature size reduction.

[0006] "Pitch doubling" or "pitch multiplication" is one method for extending the capabilities of photolithographic techniques beyond their minimum pitch. A pitch multiplication method is illustrated in Figures 1A-1F and described in U.S. Patent No. 5,328,810, issued to Lowrey *et al.*, the entire disclosure of which is incorporated herein by reference. With reference to Figure 1A, a pattern of lines 10 is photolithographically formed in a photoresist layer, which overlies a layer 20 of an expendable material, which in turn overlies a substrate 30. As shown in Figure 1B, the pattern is then transferred using an etch (preferably an anisotropic etch) to the layer 20, thereby forming placeholders, or mandrels, 40. The photoresist lines 10 can be stripped and the mandrels 40 can be isotropically etched to increase the distance between neighboring mandrels 40, as shown in Figure 1C. A layer 50 of spacer material is subsequently deposited over the mandrels 40, as shown in Figure 1D. Spacers 60, *i.e.*, the material extending or originally formed extending from sidewalls of another material, are then formed on the sides of the mandrels 40. The spacer formation is accomplished by performing a spacer etch, *i.e.*, by preferentially, directionally etching the spacer material from the horizontal surfaces 70

and 80, as shown in Figure 1E. The remaining mandrels 40 are then removed, leaving behind only the spacers 60, which together act as a mask for patterning, as shown in Figure 1F. Thus, where a given pitch previously included a pattern defining one feature and one space, the same width now includes two features and two spaces, with the spaces defined by, *e.g.*, the spacers 60. As a result, the smallest feature size possible with a photolithographic technique is effectively decreased.

[0007] While the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling," or, more generally, pitch "multiplication." Thus, conventionally, "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein.

[0008] It will be appreciated that etch processes may remove different parts of a surface at different rates. For example, the trim etch of the mandrels 40 may etch the sidewalls of the mandrels 40 at varying rates across a substrate, due to local differences in temperatures that can cause local differences in etch rates. These non-uniformities can then be transferred to the spacers 60 formed on the sidewalls and, ultimately, lead to non-uniformities in features patterned in the substrate 30 using the spacers 60.

[0009] Moreover, the materials used to form the mandrels 40 should typically be compatible with various process steps, *e.g.*, the materials are typically materials for which a suitable selective isotropic etch is available (to perform the trim etch) and for which suitable selective anisotropic etches are available for various pattern formation and pattern transfer steps (*e.g.*, for transferring patterns from overlying resist). In turn, the material for the mandrels 40 can limit the choice of later-deposited materials, *e.g.*, spacer materials, since the deposition conditions for the later-deposited materials should typically not adversely affect the mandrels 40. The requirement of the isotropic etch, in addition to the other requirements for compatible etches and deposited materials, can limit the choice of materials used in pitch multiplication, thereby limiting process latitude.

[0010] Accordingly, there is a need for methods for extending the capabilities of pitch multiplication.

SUMMARY OF THE INVENTION

[0010] According to one aspect of the invention, a method is provided for semiconductor processing. The method comprises providing a temporary feature over a substrate. The temporary feature comprises a first material. The first material is reacted with a chemical species to form a mask feature comprising the product of the reaction between the first material and the chemical species. Unreacted first material is subsequently selectively removed.

[0011] According to another aspect of the invention, a method is provided for semiconductor processing. The method comprises forming a plurality of temporary placeholders formed of temporary material across a region over a substrate. The temporary placeholders are separated by spaces. Some of the temporary material is converted into an other material to form a plurality of spacers. The other material forms a plurality of mask features. Unconverted temporary material is selectively removed. The substrate is processed through a mask pattern defined by the plurality of spacers.

[0012] According to another aspect of the invention, a method is provided for forming an array of repeating features in an integrated circuit. The method comprises lithographically defining a plurality of resist features in a resist layer over a substrate to form a pattern. The resist features each have a width defined by lithographically. The pattern is transferred to a layer of mandrel material under the resist layer to form a plurality of mandrels on a level over the substrate. The mandrels each have a width substantially equal to a width of the resist features. A plurality of spacers is formed on the level of the mandrels without etching the mandrels after transferring the pattern. The distance between the spacers is less than the width of the mandrels. The pattern defined by the spacers is transferred to the substrate to form the array of repeating features.

[0013] According to yet another aspect of the invention, a method is provided method for fabricating an integrated circuit. The method comprises providing a mandrel in a region of the integrated circuit. A layer of material is deposited over the mandrel. The layer of material is isotropically etched to leave exposed spacers at the sides of the mandrel.

[0014] According to another aspect of the invention, an intermediate mask pattern overlying a partially fabricated integrated circuit is provided. The mask pattern comprises a plurality of spaced mandrels, which each have a cap layer overlying its top

surface. A layer of pre-spacer material overlies each cap layer. The partially fabricated integrated circuit further comprises spacers on sides of each of the mandrel. The spacers comprise a combination of the pre-spacer material and the mandrel material. The pre-spacer material also extends between neighboring spacers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The invention will be better understood from the Detailed Description of the Preferred Embodiments and from the appended drawings, which are meant to illustrate and not to limit the invention, and wherein:

[0016] Figures 1A-1F are schematic, cross-sectional side views of a sequence of masking patterns for forming conductive lines, in accordance with a prior art pitch doubling method;

[0017] Figure 2 is a schematic cross-sectional side view of a partially formed integrated circuit, in accordance with preferred embodiments of the invention;

[0018] Figure 3 is a schematic cross-sectional side view of the partially formed integrated circuit of Figure 2 after forming features in a photoresist layer, in accordance with preferred embodiments of the invention;

[0019] Figure 4 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 3 after etching through a hard mask layer, in accordance with preferred embodiments of the invention;

[0020] Figure 5 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 4 after transferring a pattern from the hard mask layer to a layer of mandrel material to form a pattern of mandrels in the temporary layer, in accordance with preferred embodiments of the invention;

[0021] Figure 6 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 5, after depositing a layer of a pre-spacer material, in accordance with preferred embodiments of the invention;

[0022] Figure 7 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 6 after reacting the layer of the pre-spacer material to form spacers on the mandrel sidewalls, in accordance with preferred embodiments of the invention;

[0023] Figure 8 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 7 after selectively removing unreacted pre-spacer material, in accordance with preferred embodiments of the invention;

[0024] Figure 9 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 8 after removing a hard mask layer, in accordance with preferred embodiments of the invention;

[0025] Figure 10 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 9 after selectively removing unreacted mandrel material, in accordance with preferred embodiments of the invention;

[0026] Figure 11 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 10 after transferring a pattern formed by the spacers to a hard mask layer underlying the spacers, in accordance with preferred embodiments of the invention;

[0027] Figure 12 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 11 after removing the spacers, in accordance with preferred embodiments of the invention;

[0028] Figure 13 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 12 after transferring the pattern in the masking layer to an underyling substrate, in accordance with preferred embodiments of the invention

[0029] Figure 14 is a schematic, cross-sectional side view of a partially formed integrated circuit having hard a mask and additional masking layers disposed between the spacers and the substrate, in accordance with preferred embodiments of the invention;

[0030] Figure 15 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 14 after transferring the spacer pattern into the additional masking layers and an underyling substrate, in accordance with preferred embodiments of the invention; and

[0031] Figure 16 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 5 after forming spacers on sides of the mandrels by a gas phase reaction, in accordance with some preferred embodiments of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] In preferred embodiments of the invention, in a masking process, mask features, such as spacers, are formed by a reaction with a temporary feature, such as a mandrel. Preferably, the spacers are formed at the sides of mandrels and a trim etch of the mandrels is not needed. The mandrels are preferably reacted with at least one other material or chemical species to form the spacers, which comprise spacer material that is a product of the reaction. A cap layer is preferably formed over the top, horizontal surface of the mandrels to inhibit reactions on that surface. Thus, the reactions preferably occur at the sides of the mandrels and convert the sidewall mandrel material into spacer material. Unreacted mandrel material is then preferably removed, to leave a pattern of free-standing spacers. Preferably, the spacers are formed without a spacer etch, *i.e.*, without performing a directional etch that preferentially removes spacer material from horizontal surfaces. After removing the mandrel material, the pattern of free-standing spacers can be used in a mask for subsequently processing an underlying substrate.

[0033] The conversion of mandrel material into spacer material can be accomplished by various processes, including, *e.g.*, oxidation, nitridation, silicidation and polymerization. For example, a layer of a material is formed on the sides the mandrels (*e.g.*, by performing a conformal blanket deposition over the mandrels) and the mandrels are made to react with that layer of material by, *e.g.*, performing an anneal. In other embodiments, the mandrels can be exposed to one or more gaseous reactants to form the spacer material, or the mandrels can be exposed to energy (*e.g.*, light) or other agents (*e.g.*, catalysts) to convert the exposed mandrel material into another material by, *e.g.*, polymerizing or cross-linking the exposed sidewalls of the mandrel material.

[0034] Advantageously, because the spacers are formed by converting part of the mandrels into spacer material, a trim of the mandrels is not necessary. The spacers are formed extending into the mandrels and, thus, can be made closer together than would be the case if the spacers were formed on the sidewalls of the mandrels. The extent of the spacer formation reaction can influence both the thickness of the spacers and the spacing therebetween. Advantageously, the spacer separation can be similar to the separation achieved after performing a mandrel trim etch in a typical pitch multiplication process. Moreover, because a trim etch is not necessary, the selection of materials for the mandrel is not limited to materials compatible with the trim etch. In addition, a spacer etch can

advantageously be avoided. It will be appreciated that a spacer etch can round the top edges of a spacer. Such rounding can be undesirable as it, *e.g.*, effectively reduces the aspect ratio of the spacers and/or encourages an uneven distribution of etchants or other materials during application of etchants or other material to any layers underlying the spacers. Advantageously, spacers formed according the preferred embodiments can have a more uniform, square shape. Moreover, a spacer etch can be more aggressive and can erode underlying material to a greater extent than the removal of unreacted material in the preferred embodiments.

[0035] Reference will now be made to the Figures, wherein like numerals refer to like parts throughout. It will be appreciated that the Figures are not necessarily drawn to scale.

[0036] Initially, a sequence of layers of materials is formed to allow formation of spacers over a substrate.

[0037] Figure 2 shows a cross-sectional side view of a partially formed integrated circuit 100. While the preferred embodiments can be used to form any integrated circuit, they are particularly advantageously applied to forming devices having repeating patterns or arrays of electrical devices, including memory cell arrays for volatile and non-volatile memory devices such as DRAM, phase change RAM, programmable conductor (PCRAM), ROM or flash memory, including NAND flash memory, or integrated circuits having logic or gate arrays. For example, the logic array can be a field programmable gate array (FPGA) having a core array similar to a memory array and a periphery with supporting logics. Consequently, the integrated circuit 100 can be, *e.g.*, a memory chip or a processor, which can include both a logic array and embedded memory, or any other integrated circuit having a logic or a gate array.

[0038] With continued reference to Figure 2, various masking layers 120-150 are preferably provided above a substrate 110. It will be appreciated that the substrate 160 can be a silicon wafer or any structure or layer of material overlying a wafer. For example, the substrate 100 can comprise an insulating film.

[0039] The layers 120-150 will be etched to form a mask for patterning the substrate 110, as discussed below. Materials for the layers 120-150 are preferably chosen based upon consideration of the chemistry and process conditions for the various pattern forming and pattern transferring steps discussed herein. Because the layers between a topmost selectively definable layer 120 and the substrate 110 preferably function to

transfer a pattern derived from the selectively definable layer 120 to the substrate 110, the layers 130-150 between the selectively definable layer 120 and the substrate 110 are preferably chosen so that they can be selectively etched relative to other exposed materials at various stages, as described below. It will be appreciated that a material is considered selectively, or preferentially, etched when the etch rate for that material is at least about 5 times greater, preferably at least about 10 times greater, more preferably at least about 20 times greater and, most preferably, at least about 40 times greater than that for surrounding materials. Because a goal of the layers 120-150 overlying the substrate 110 is to allow well-defined patterns to be formed in that substrate 110, it will be appreciated that one or more of the layers 120-150 can be omitted or substituted if suitable other materials, chemistries and/or process conditions are used. For example, an antireflective coating can be formed between the layers 120 and 130 in some embodiments where the resolution enhancement properties of such a layer are desired. In other embodiments, discussed further below, additional masking layers can be added between the layer 150 and the substrate 110 to form a mask having improved etch selectivity relative to the substrate 110. Optionally, if appropriate etch chemistries are available, the layer 150 can be omitted and the spacers 175 (Figure 10) can be used as a mask to, *e.g.*, pattern the substrate without any intervening materials. Exemplary materials for the various layers discussed herein include silicon oxide, silicon nitride, silicon, amorphous carbon, dielectric antireflective coatings (DARC, silicon rich silicon oxynitride), and organic bottom antireflective coatings (BARC), each of which can be selectively etched relative to at least 2 or 3 of the other materials, depending upon the application.

[0040] In addition to selecting appropriate materials for the various layers, the thicknesses of the layers 120-150 are preferably chosen depending upon compatibility with the etch chemistries and process conditions described herein. For example, when transferring a pattern from an overlying layer to an underlying layer by selectively etching the underlying layer, materials from both layers are removed to some degree. Preferably, the upper layer is thick enough so that it is not worn away over the course of the pattern transfer.

[0041] The selectively definable layer 120 preferably overlies a hard mask layer 130, which preferably can function as a cap layer to shield mandrels 145 (Figure 5) from reactive agents, as discussed below. The layer 130 overlies a mandrel layer 140, which overlies a second hard mask, or etch stop, layer 150, which overlies the substrate

110 to be processed (*e.g.*, etched) through a mask. The selectively definable layer 120 is preferably photodefinable, *e.g.*, formed of a photoresist, including any photoresist known in the art. For example, the photoresist can be any photoresist compatible with 157 nm, 193 nm, 248 nm or 365 nm wavelength systems, 193 nm wavelength immersion systems, extreme ultraviolet systems (including 13.7 nm wavelength systems) or electron beam lithographic systems. In addition, maskless lithography, or maskless photolithography, can be used to define the selectively definable layer 120. Examples of preferred photoresist materials include argon fluoride (ArF) sensitive photoresist, *i.e.*, photoresist suitable for use with an ArF light source, and krypton fluoride (KrF) sensitive photoresist, *i.e.*, photoresist suitable for use with a KrF light source. ArF photoresists are preferably used with photolithography systems utilizing relatively short wavelength light, *e.g.*, 193 nm. KrF photoresists are preferably used with longer wavelength photolithography systems, such as 248 nm systems. In other embodiments, the layer 120 and any subsequent resist layers can be formed of a resist that can be patterned by nano-imprint lithography, *e.g.*, by using a mold or mechanical force to pattern the resist.

[0042] The material for the hard mask layer 130 preferably comprises an inorganic material. Exemplary materials include, without limitation, silicon oxide and silicon nitride. In the illustrated embodiment, the hard mask layer 130 comprises silicon nitride. The mandrel layer 140 is preferably formed of a material that can be converted into a spacer material, which in turn offers good etch selectivity relative to the unreacted mandrel material, the hard mask layer 130 and material underlying the spacer material. In the illustrated embodiment, the mandrel material is silicon.

[0043] The material for the second hard mask layer 150 is preferably chosen based upon the material used for the spacers 175 (Figure 11) and for the underlying substrate 110. Where the layer 150 is used as a mask to etch the substrate 110, the layer 150 is preferably formed of a material that is resistant to the desired processing (*e.g.*, etching, doping, oxidizing, etc.) of the substrate 110 to be conducted through the mask and can be selectively etched relative to the spacers 175 (Figure 11). For example, the second hard mask layer 150 can be a nitride, *e.g.*, silicon nitride, or can be an oxide, *e.g.*, silicon oxide. In the illustrated embodiment, the second hard mask layer 150 comprises silicon oxide.

[0044] The various layers discussed herein can be formed by various methods known in the art. For example, spin-on-coating processes can be used to form

photodefinable layers, BARC, and spin-on dielectric oxide layers. Various vapor deposition processes, such as sputtering, chemical vapor deposition (CVD) and/or atomic layer deposition (ALD), can be used to form various hard mask, cap and mandrel layers. In addition, some layers, *e.g.*, the layer 140, can be reacted to form other layers. For example, rather than depositing a silicon nitride layer using silicon and nitrogen precursors, the top surface of the silicon layer 140 can be nitrided using a nitrogen precursor to form a silicon nitride layer, which can serve as a hard mask layer, or a cap layer for the subsequently produced mandrel (as will be better understood in view of the discussion below).

[0045] Having formed a desired stack of layers, a pattern of spacers is next formed.

[0046] With reference to Figure 3, a pattern comprising spaces or trenches 122, which are delimited by features 124 formed of photodefinable material, is formed in the photodefinable layer 120. The trenches 122 can be formed by, *e.g.*, photolithography with 248 nm or 193 nm light, in which the layer 120 is exposed to radiation through a reticle and then developed. The remaining photodefined material forms mask features such as the illustrated lines 124 (shown in cross-section only) after being developed. Advantageously, the lines 124 can be formed having widths of about 120 nm or less, or about 80 nm or less, to form spacers having a pitch of about 100 nm or less.

[0047] With reference to Figure 4, the pattern of photoresist features 124 and trenches 122 is transferred to the hard mask layer 130. This transfer is preferably accomplished using an anisotropic etch, such as an etch using a CF_4, CF_4/H_2, CF_4/O_2, SF_6 or NF_3-containing plasma, although a wet (isotropic) etch may also be suitable if the hard mask layer 130 is sufficiently thin to be etched through without undesirably widening spaces in the transferred pattern.

[0048] With reference to Figure 5, the pattern in the photodefinable layer 120 and the hard mask layer 130 is transferred to the mandrel layer 140 to form mandrels, or temporary placeholders, 145. The transfer is preferably accomplished using an anisotropic etch employing, *e.g.*, HBr/HCl or $CHCl_3/Cl_2$-containing plasma. The widths of the mandrels 145 are preferably substantially similar to the widths of the lines 124, *e.g.*, the mandrels 145 preferably have a width of about 120 nm of less, or about 80 nm or less.

[0049] With reference to Figure 6, pre-spacer material, *i.e.*, material to be reacted to form spacers, is deposited on the sidewalls of the mandrels 145. Preferably, the

pre-spacer material is blanket deposited as a layer 170 on the mandrels 145. In the illustrated embodiment, the pre-spacer material that forms the layer 170 is titanium. The deposition can be accomplished by various methods known in the art, including, *e.g.*, CVD and ALD. The thickness of the layer 170 is preferably chosen to provide sufficient material to form spacers 175 (Figure 7) of the desired width after reaction of the pre-spacer material 170 with the mandrels 145, as discussed below.

[0050] With reference to Figure 7, the titanium pre-spacer layer 170 and the mandrels 145 are next reacted with one another to form spacers 175, composed of a titanium silicide in the illustrated embodiment. It will be appreciated that the mandrels 145 are preferably provided with a cap layer to focus the reaction on the sidewalls of the mandrels 145. In the illustrated embodiment, the hard mask layer 130 preferably acts as the cap layer to prevent the top of the mandrels 145 from being reacted, by preventing contact between the titanium pre-spacer layer 170 and the top surface of the mandrels 145. In other embodiments, the cap layer can be separately formed, *e.g.*, by deposition on or reaction of the top of the mandrels 145, whether or not the hard mask layer 130 is present.

[0051] Preferably, the layer 170 and the mandrels 145 are subjected to an elevated temperature, *e.g.*, an anneal, to cause a self-aligned silicidation reaction. For example, the partially fabricated integrated circuit 100 can be subjected to rapid thermal processing (RTP) at a temperature of about 550-800°C, more preferably, about 650-680°C, for about 5-90 seconds, more preferably, about 20-60 seconds.

[0052] It will be appreciated that the extent of the reaction and the amount of titanium in the layer 170 that reacts with the silicon of the mandrels 145 is related to the temperature and duration of the anneal. Thus, advantageously, reaction conditions, such as the temperature and duration of the anneal, can be selected depending upon the width and/or separation distance desired for the spacers 175. For example, the mandrels 145 and the layer 170 can be reacted until the separation is about 80 nm or less or, more preferably, about 50 nm or less.

[0053] In other embodiments, the parts of the titanium layer 170 at the sidewalls of the mandrels 145 are preferably fully reacted. Advantageously, fully reacting these parts allows for a larger process window for the anneal and good control over the widths of the spacers 175, since the thickness of the layer 170 typically places a limit on the maximum width of the spacers 175 formed by the reaction. For example, by

depositing the layer 170 to a given width, the duration and/or temperature of the anneal can be allowed to exceed the duration and/or temperature needed to form spacers 175 of that width, since the amount of material (*e.g.*, the width) of the layer 170 typically limits the growth of the spacers 175, particularly in the direction of the layer 170.

[0054] With reference to Figure 8, unreacted titanium in the layer 170 is selectively removed to leave the spacers 175 at the sides of the mandrels 145. The removal can be accomplished by wet or dry etches. A wet etch can have advantages for reduced costs and less damage to the structure of the spacers 175. An example of a suitable etch is a wet etch comprising H_2O, H_2O_2 and NH_4OH. Preferably, the spacers 175 are sublithographic, *i.e.*, they have a critical dimension, *e.g.*, width, that is below the resolution limit of the photolithographic technique used for forming the spacer pattern, in this case, the photolithographic technique used to pattern the layer 120.

[0055] With reference to Figure 9, the silicon nitride cap layer 130 is selectively removed relative to the spacers 175. This removal can be accomplished using a dry etch or a wet etch, *e.g.*, using hot phosphoric acid.

[0056] Next, as shown in Figure 10, unreacted mandrel material is selectively removed to form a pattern of free-standing spacers 175. Dry or wet etches can be employed for this removal. An exemplary wet etch comprises HF, HNO_3 and H_2O. A hard mask layer 150 can be provided underlying the spacers 175, to protect the substrate 110 and to allow unreacted mandrel material to be removed without unintentionally removing material in the substrate 110. Thus, advantageously, the spacers 175 can be formed having a pitch that is roughly half that of the photoresist lines 124 and spaces 122 (Figure 3) originally formed by photolithography. Where the photoresist lines 124 had a pitch of about 200 nm, spacers 175 having a pitch of about 100 nm or less can be formed.

[0057] It will be appreciated that because the spacers 175 are formed in the sidewalls of the mandrels 145, the spacers 175 generally follow the outline of the mandrels 145 and, so, typically form a closed loop. It will be appreciated that where the pitch multiplied pattern is used to form features such as conductive lines, additional processing steps can be used to cut off or otherwise prevent transfer of the pattern at the ends of these loops, so that each loop forms two individual, non-connected lines. This can be accomplished, for example, by depositing a layer of a protective material over the loops, patterning the protective layer to form a protective mask around the parts of the lines to be maintained, and then etching away the unprotected parts, *e.g.*, the ends, of the

loops. A suitable method for cutting off the ends of the loops is disclosed in U.S. Patent Application No. 10/931,771 to Tran *et al.*, filed August 31, 2004, the entire disclosure of which is incorporated be reference herein.

[0058] With reference to Figure 11, in addition to protecting the substrate 110 during a spacer removal, the hard mask layer 150 preferably allows for improved etch selectivity relative to the substrate 110, in cases where the pattern of spacers 175 is to be transferred to the substrate 110. As discussed above, the hard mask layer 150 is formed of silicon oxide in the illustrated embodiment. The pattern of spacers 175 is preferably transferred to the layer 150 using an anisotropic etch, *e.g.*, an etch containing CHF_3, CF_4 or C_2F_6 plasma. If the hard mask layer 150 is sufficiently thin, it will be appreciated that a wet etch may also be used to accomplish the pattern transfer with minimal undercutting.

[0059] Next, the hard mask layer 150 can be used to pattern the underlying substrate 110.

[0060] It will be appreciated that the spacers 175 can be removed before or after etching the substrate 110. Preferably, where the material of the hard mask layer 150 offers good etch selectivity relative to the material of the substrate 110, *e.g.*, where the spacers 175 are not needed to supplemental the hard mask layer 150, the spacers 175 can be removed before the pattern is transferred to the substrate 110. The spacer removal can be accomplished using, *e.g.*, a dilute HF wet etch. Advantageously, the spacer removal reduces the aspect ratio of the spaces through which processing is conducted, *e.g.*, through which etchants must travel to reach the substrate 110 and minimizes the possibility of alterations in the pattern caused by collapse or deformation of the spacers 175, especially where the spacers 175 are very tall and/or narrow. Thus, as shown in Figure 11, the spacers 175 can be removed to facilitate the etch of the substrate.

[0061] With reference to Figure 13, the pattern in the hard mask layer 150 can be transferred to the substrate 110 using, *e.g.*, an etch or combination of etches selective for the material(s) of the substrate 110. In addition to etching the substrate through masks, in other embodiments, other types of processing through the mask in the layer 150 are also possible. Non-limiting examples of other processes include implantation, diffusion doping, lift-off patterned deposition, oxidation, nitridation, etc.

[0062] With reference to Figure 14, in other embodiments, especially where the substrate 110 is difficult to etch or where prolonged processing through the mask is desired, one or more additional intervening layers of masking material can be formed

between the spacers 175 and the substrate 110. For example, an additional layer 160 can be provided, as discussed in co-pending U.S. Patent Provisional Application No. 60/662,323 to Tran *et al.*, filed March 15, 2005, entitled Pitch Reduced Patterns Relative To Photolithography Features, Attorney Docket No. MICRON.316PR (Micron Ref. No. 2004-1130.00/US), the entire disclosure of which is incorporated herein by reference.

[0063] With continued reference to Figure 14, the layer 150 preferably comprises a material that has good etch selectively relative to the spacers 175, the layer 160 and the mandrels 145 (Figure 9). The layer 160 is preferably formed of amorphous carbon, which is advantageously resistant to many etch chemistries for removing silicon materials in the substrate 110.

[0064] With reference to Figure 15, the pattern defined by the spacers 175 can be transferred to the layer 160, which then serves as the primary mask 160 for patterning the substrate 110. Advantageously, in other embodiments, due to the availability of extreme selectivity when etching amorphous carbon, a patterned hard mask layer 150 can be used to transfer the pattern from the layer 150 to the layer 160 after removal of the spacers 175, so that the mask used to transfer the pattern to the primary masking layer 160 has lower and more uniform aspect ratio features. In other embodiments, in conjunction with suitable other materials, the hard mask layer 150 can itself be formed of amorphous carbon.

[0065] In yet other embodiments, there may be no intervening layers, *e.g.*, no hard mask layer 150, between the substrate 110 and the spacers 175. In such cases, especially where the spacer material has good etch selectivity relative to the substrate, the substrate 110 can be processed through the pattern of spacers 175 without any intervening hard mask layers.

[0066] It will be appreciated that the formation of spacers according to the preferred embodiments offers numerous advantages. For example, a mandrel trim etch is not necessary and the spacer non-uniformities that can be caused by such a trim etch can be eliminated. Instead, deposition of the pre-spacer layer 170 and the extent of a spacer formation reaction, *e.g.*, an anneal, determine both the spacer width and the spacer spacing. Moreover, because a trim etch is not performed, the range of materials that can be used to form mandrels may be expanded, as requirements for compatibility with trim etches is removed. Thus, processing flexibility can be increased. In addition, a directional spacer etch is not necessary, allowing advantages with respect to forming

spacers 175 with symmetrically shaped shoulders and to minimizing damage to underlying layers.

[0067] While a spacer etch is advantageously not necessary in the preferred embodiments, in some arrangements, a spacer etch can be performed on the layer 170 of pre-spacer material to form spacer features, formed of pre-spacer material, on the sides of the mandrels before reacting the pre-spacer material and the mandrel material. These spacer features can then be reacted with the mandrel material to form the spacers 175, which are selectively etchable relative to the mandrel material and underlying materials.

[0068] It will also be appreciated that, while discussed with reference to particular processing steps and materials in the illustrated embodiment, various modifications are possible. For example, various silicides in addition to titanium silicide can be used to form the spacers. Examples of other metals to form metal silicides include tantalum, hafnium, and nickel. In the example above, these metals can be deposited over the mandrels and annealed to form a metal silicide. In other arrangements, the combination of materials can be reversed. For example, the mandrels 145 can be metallic and a silicon layer is deposited over the mandrels to form a metal silicide. In addition, the mandrels 145 can comprise amorphous carbon and the layer 170 can comprise various other materials reactive with amorphous carbon. For example, the layer 170 can comprise silicon to form silicon carbide spacers 175, or the layer 170 can comprise a metal to form a metal carbide.

[0069] With reference to Figure 16, it will be appreciated that while the formation of the spacers 175 is illustrated as a solid state reaction in which a deposited metal layer reacts with the mandrels, the spacers 175 can be formed by various processes other than reactions between solid state reactants. In some embodiments, the mandrels 145 can be reacted with a gaseous reactant to form spacers, including spacers that are not silicides. For example, a silicidation of a silicon mandrel 145 can be accomplished by exposing the mandrels 145 to a gaseous metal reactant (*e.g.*, $TiCl_4$, WF_6, etc.), or a gas phase silicidation of a metal mandrel 145 can be accomplished by exposing the mandrels 145 to a gaseous silicon reactant (*e.g.*, SiH_4). In addition, silicon oxide spacers can be formed by exposing silicon mandrels to an oxidant or, where the cap layer is a suitable material other than silicon nitride, silicon nitride can be formed by exposing silicon mandrels to a reactive nitrogen species. In other embodiments, the mandrels 145 can be a carbon species, such as amorphous carbon, resist, or carbon-doped materials (*e.g.*, as

disclosed in U.S. Patent No. 6,515,355, the entire disclosure of which is incorporated by reference herein) which is converted to a polymer or cross-linked to form spacers 175. The conversion can be caused by exposure to energy (*e.g.*, light) or other agents (*e.g.*, catalysts). After the spacers 175 are formed, the partially fabricated integrated circuit 100 can be processed as discussed above regarding Figures 9-15.

[0070] Additionally, while two materials are discussed above for ease of illustration and description, it will be appreciated that more than two materials can be reacted to form a desired spacer material, *e.g.*, SiO_xN_y formed by a reaction with gas phase reactants. These additional materials can be reacted by, *e.g.*, forming depositing multiple layers of pre-spacer materials over one another and then performing an anneal and/or by depositing a single layer of pre-spacer material, performing an anneal to react that layer with the mandrel material and then depositing one or more additional layers of pre-spacer material and then performing an anneal. In other embodiments, the additional materials can be introduced as gaseous reactants as an alternative to or in additional to depositing layers of pre-spacer material.

[0071] Moreover, while trim etches are preferably not performed in the formation of the mandrels, a trim etch can be performed if desired. For example, the photoresist layer can be subjected to a trim etch after being developed, and/or the mandrels can be subjected to a trim etch. Such a trim etch may be useful to form spacers that are exceptionally close to together.

[0072] Additionally, the cap layer can be formed after forming the mandrels. For example, the tops of the mandrels may be reacted with directionally applied reactants, *e.g.*, in a process similar to ion implantation, to form the cap layer.

[0073] Moreover, the spacers are formed without a cap layer for the mandrels. For example, a metal layer can be conformally deposited over the mandrels and both the top and sides of the mandrels can be reacted. The reacted top parts can them be removed, *e.g.*, by a directional dry etch or by filling the empty spaces between the mandrels with a filler material, performing chemical mechanical polishing to remove the top parts and then removing the filler material.

[0074] As with the spacers, it will also be appreciated that other materials can be used for the various other layers and parts discussed herein. Preferably, any other materials that may be used offer the appropriate etch selectivity relative to the materials that are exposed during the selective etch steps, as discussed above. Moreover, the

substrate 110 can comprise different materials, *e.g.*, layers of different materials, or different materials in different lateral regions of the substrate. To transfer the pattern defined by the spacers to such a substrate, a succession of different chemistries, preferably dry-etch chemistries, can be used to successively etch through these different materials, if a single chemistry is not sufficient to etch all the different materials.

[0075] It will also be appreciated that, depending upon the chemistry or chemistries used, overlying spacers and hard mask layers may be etched. In some cases, the additional masking layer 160 (Figure 14) is preferably used for superior etch selectivity. Using amorphous carbon for the primary mask layer 160 advantageously offers excellent resistance to conventional etch chemistries, especially those used for etching silicon-containing materials. Thus, the primary mask layer 160 can effectively be used as a mask for etching through a plurality of substrate layers, or for forming high aspect ratio trenches.

[0076] Also, the masks discussed herein can be used to form various integrated circuit features, including, without limitation, conductive interconnect lines, landing pads and parts of various electrical devices, such as capacitors and transistors, particularly for memory and logic arrays, or flat panel displays, in which dense repeating patterns are desirable. As such, while illustrated as lines with regular spacing and regular widths for ease of illustration, the masks can have features with variable spacing. Also, while illustrated with spacers formed on a single level, in other embodiments, spacers can be formed on multiple vertical levels and consolidated on a single level to form a mask pattern.

[0077] In addition, the pitch of the pattern formed in the photoresist layer 120 can be more than doubled. For example, the pattern can be further pitch multiplied by using the spacers 175 as mandrels for a conventional pitch multiplication process in which additional spacers are formed around the spacers 175, then the spacers 175 are removed, then spacers are formed around the spacers that were formerly around the spacers 175, and so on.

[0078] The preferred embodiments can also be employed multiple times throughout an integrated circuit fabrication process to form features in a plurality vertical levels, which may be vertically contiguous or non-contiguous and vertically separated. In such cases, each of the individual levels to be patterned would constitute a substrate 110. In addition, some of the preferred embodiments can be combined with other of the

preferred embodiments, or with other masking methods known in the art, to form features on different areas of the same substrate 110 or on different vertical levels.

[0079] Accordingly, it will be appreciated by those skilled in the art that these and various other omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

WE CLAIM:

1. A method for semiconductor processing, comprising:

forming a plurality of temporary placeholders formed of temporary material across a region over a substrate, the temporary placeholders separated by spaces;

forming a cap layer overlying a top surface of each of the temporary placeholders;

converting some of the temporary material into an other material to form a plurality of spacers, the other material forming a plurality of mask features, the cap layer inhibiting reactions at the top surface;

selectively removing unconverted temporary material; and

processing the substrate through a mask pattern defined by the plurality of spacers.

2. The method of Claim 1, wherein converting some of the temporary material comprises selectively reacting sidewalls of the temporary placeholders with a chemical species.

3. The method of Claim 2, wherein selectively reacting sidewalls of the temporary placeholders comprises performing an anneal, wherein selecting reaction conditions comprises selecting a temperature and duration for the anneal based upon a desired critical dimension of the mask features.

4. The method of Claim 2, wherein selectively reacting sidewalls of the temporary placeholders comprises reacting the sidewalls with a solid phase reactant by blanket depositing a layer comprising the solid phase reactant on the temporary placeholders.

5. The method of Claim 4, wherein converting some of the temporary material comprises reacting a portion of the layer comprising the solid phase reactant with the temporary material and further comprising preferentially removing an unreacted remainder of the layer.

6. The method of Claim 4, wherein the solid phase reactant comprises a metal and the other material comprises a metal silicide.

7. The method of Claim 6, wherein the metal is selected from the group consisting of titanium, tantalum, hafnium, and nickel.

8. The method of Claim 2, wherein selectively reacting sidewalls of the mandrels comprises exposing the sidewalls to a gas phase reactant.

9. The method of Claim 1, wherein forming the plurality of temporary placeholders comprises:

defining a pattern in a selectively definable layer over a substrate; and

transferring the pattern from the selectively definable layer to an underlying layer formed of the temporary material.

10. The method of Claim 9, wherein defining the pattern comprises performing photolithography.

11. The method of Claim 1, wherein selectively removing unconverted temporary material comprises performing a wet etch.

12. The method of Claim 1, wherein the temporary material comprises silicon.

13. The method of Claim 1, wherein the other material comprises a polymer.

14. A method for fabricating an integrated circuit, comprising:

providing a mandrel in a region of the integrated circuit;

depositing a layer of material over the mandrel;

isotropically etching the layer of material to leave exposed spacers at sides of the mandrel;

transferring a spacer pattern formed by the spacers to an underlying hard mask layer; and

transferring the spacer pattern from the hard mask layer to a substrate.

15. The method of Claim 14, wherein the layer of material comprises a pre-spacer material, further comprising reacting the pre-spacer material with the mandrel before isotropically etching, wherein reacting the pre-spacer material with the mandrel forms a spacer material resistant to the etch used for isotropically etching.

16. The method of Claim 17, wherein the pre-spacer material is titanium and the spacer material is titanium silicide.

17. The method of Claim 14, further comprising preferentially removing the mandrels relative to the spacers.

18. The method of Claim 14, wherein the spacers are sublithograhic features.

19. The method of Claim 14, further comprising:

depositing a layer of additional spacer material on sides of the spacers;

anisotropically etching the layer of additional spacer material to form additional spacers on sidewalls of the spacers; and

selectively removing the spacers between the additional spacers to leave a pattern of free standing additional spacers.

20. An intermediate mask pattern overlying a partially fabricated integrated circuit, comprising:

a plurality of spaced mandrels formed of a mandrel material;

a cap layer overlying a top surface of each of the mandrels;

a layer of pre-spacer material overlying each cap layer; and

spacers on sides of each of the mandrels, wherein the spacers comprise a combination of the pre-spacer material and the mandrel material, wherein the pre-spacer material extends between neighboring spacers.

21. The intermediate mask pattern of Claim 20, wherein the cap layer comprises silicon oxide or silicon nitride.

22. The intermediate mask pattern of Claim 20, wherein the mandrel comprises silicon.

23. The intermediate mask pattern of Claim 20, wherein the spacers comprise a metal silicide.

24. The intermediate mask-pattern of Claim 20, wherein the spacers are sublithographic features.

25. The intermediate mask pattern of Claim 20, wherein a width of the top surface is less than about 80 nm.

26. The intermediate mask pattern of Claim 25, wherein the spacers are separated by less than about 50 nm.