

CLOCK GENERATION CIRCUIT AND LATCH USING SAME, AND COMPUTING DEVICE

ABSTRACT

A clock generation circuit, a latch using same, and a computing device are provided. The
5 clock generation circuit includes an input end, configured to input a pulse signal (CKI); a first
output end, configured to output a first clock signal (CKO1); a second output end, configured
to output a second clock signal (CKO2); and an input drive circuit (101), a latch circuit (102),
an edge shaping circuit (103), a feedback delay unit (104), and an output drive circuit (105),
where the input drive circuit (101), the latch circuit (102), the edge shaping circuit (103), the
10 feedback delay unit (104), and the output drive circuit (105) are sequentially connected
between the input end and the first output end as well as the second output end in series. A
clock pulse can be effectively shaped, the use of a clock buffer can be reduced, and the
correctness and accuracy of data transmission and latching can be improved.

15 Fig. 5