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(54) Title: A METHOD AND APPARATUS FOR TRANSPORTING MESSAGES BETWEEN PROCESSORS IN A MULTIPLE PROCESSOR SYSTEM**(57) Abstract**

A message unit (210) that provides a hardware queue interface between a host processor and a local processor handling I/O operations in an I/O platform. Circuitry (214) manages the head and tail pointers of an inbound free queue, an inbound post queue, an outbound free queue, and an outbound post queue. Circuitry is also provided for enabling a host processor or bus agent to access these queues in a single bus transaction by reading or writing inbound port registers or outbound port registers. The queue elements contain handles of message buffers. The invention automatically performs the specific task of locating the next element in a queue, altering that element, and modifying a queue descriptor (i.e., a head or a tail pointer) to indicate the next element for a next queue access. A plurality of registers are used for selectively interrupting either the host processor or the local processor when the queues are written to by either the host processor, a bus agent, or the local processor.

