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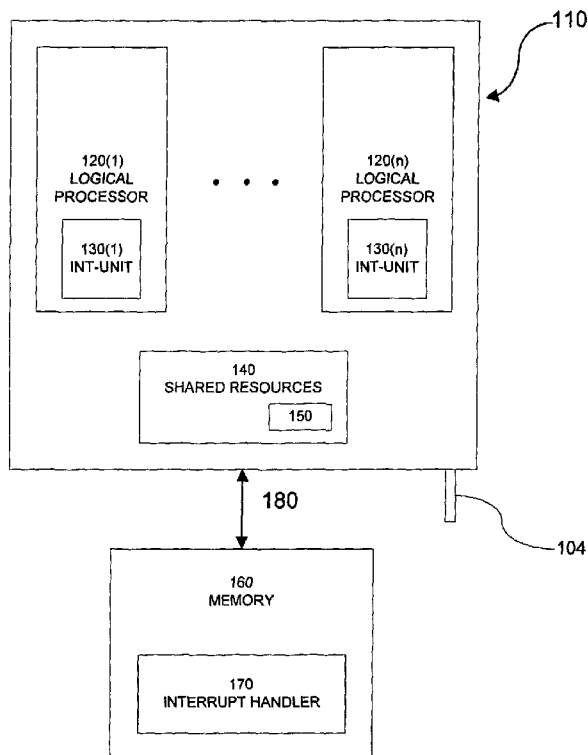
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(54) **Title: MECHANISM FOR INTERRUPT HANDLING IN COMPUTER SYSTEMS THAT SUPPORT CONCURRENT EXECUTION OF MULTIPLE THREADS**

(57) **Abstract:** The present invention provides a mechanism for handling interrupts on a processor that supports multiple-threads concurrently. The processor's resources are allocated to provide multiple logical processors. In response to a common interrupt, the logical processors vie for access to a shared register. The first logical processor to access the shared register handles the common interrupt. The remaining logical processors return from the interrupt.



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