

ABSTRACT

A nonvolatile memory device includes N planes each comprising a plurality of memory blocks, N discharge control circuits adjacent to
5 the N planes, respectively, and configured to connect each common source line of the N planes and a ground voltage terminal in response to each one of N discharge control signals, a plane selection circuit configured to select K planes of the N planes, and an operation control circuit configured to adjust voltage levels of K discharge control signals
10 according to a distance difference between the ground voltage terminal and each of K discharge control circuits corresponding to the K planes, among the N discharge control circuits.

FIG. 1