CONTROL SCHEME FOR SHARED-USE DUAL-PORT PREDICTED ERROR ARRAY

ABSTRACT

An MPEG2 compliant digital video encoder system is disclosed having a refinement processor for reconstructive processing for I-picture and P-picture encoding. The refinement processor includes a frame difference unit (1000) which has a predicted error array (PE array). The predicted error array comprises a shared-use array for storing both luminance data and chrominance data of a macroblock of data. The predicted error array also comprises a dual-port structure and array read control logic which allows simultaneous reading and writing of data to the array. Address selector logic controls addressing of the PE array such that writing of luminance data and chrominance data to the PE array and reading of luminance data and chrominance data from the array remains synchronous.

Figure 1

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