GENERATING INTEGRATED CIRCUIT FLOORPLANS USING NEURAL NETWORKS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to U.S. Patent Application No. 62/775,284, filed December 4, 2018, the entire contents which are incorporated by reference.

BACKGROUND

This specification relates to using neural networks for electronic design automation and, more specifically, for generating a computer chip floorplan.

Computer chip floorplans are schematic representations of the placement of some or all of the circuits of a computer chip on the surface, i.e., the chip area, of the computer chip.

Neural networks are machine learning models that employ one or more layers of nonlinear units to predict an output for a received input. Some neural networks include one or more hidden layers in addition to an output layer. The output of each hidden layer is used as input to the next layer in the network, i.e., the next hidden layer or the output layer. Each layer of the network generates an output from received inputs in accordance with current values of a respective set of parameters.

SUMMARY

This specification describes a system implemented as computer programs on one or more computers in one or more locations that generates a chip floorplan for an integrated circuit. The integrated circuit for which the chip floorplan is being generated will be referred to in this specification as a "computer chip" but should generally be understood to mean any collection of electronic circuits that are fabricated on one piece of semiconductor material. The chip floorplan places each node from a netlist of nodes at a respective location on the surface of the computer chip.

According to a first aspect of the present invention, there is provided a method performed by one or more computers, the method comprising:

obtaining netlist data for a computer chip, wherein the netlist data specifies a connectivity on a computer chip between a plurality of nodes that each correspond to one or more of a plurality of integrated circuit components of the computer chip; and

generating a computer chip floorplan that places each node in the netlist data at a respective position on the surface of the computer chip, comprising placing a respective node at each time step in a sequence comprising a plurality of time steps, the placing comprising, for each particular time step of the plurality of time steps:

generating an input representation for the particular time step that comprises (i) partially placed chip data characterizing a partially placed chip that indicates the placement of the nodes that have already been placed at time steps preceding the particular time step in the sequence and (ii) current node data characterizing the node to be placed at the particular time step;

processing the input representation using a node placement neural network having a plurality of network parameters, wherein the node placement neural network is configured to process the input representation in accordance with current values of the network parameters to generate a score distribution over a plurality of positions on the surface of the computer chip; and

assigning the node to be placed at the particular time step to a position from the plurality of positions using the score distribution.

According to a second aspect of the present invention, there is provided one or more computer-readable storage media storing instructions that when executed by one or more computers cause the one or more computers to perform the respective operations of the method as defined in the first aspect.

According to a third aspect of the present invention, there is provided a system comprising one or more computers and one or more storage devices storing instructions that when executed by one or more computers cause the one or more computers to perform the respective operations of the method as defined in the first aspect.

According to a fourth aspect of the present invention, there is provided a method of producing a computer chip, comprising generating a computer chip floorplan by the method as defined in the first aspect, and fabricating a computer chip according to the generated computer chip floorplan.

Particular embodiments of the subject matter described in this specification can be implemented so as to realize one or more of the following advantages.

Floorplanning, which involves placing the components of a chip on the surface of the chip, is a crucial step in the chip design process. The placement of the components should optimize metrics such as area, total wire length and congestion. If a floorplan