

Programmable digital tone detector

The invention relates to a programmable system for signaling the presence of a predetermined tone frequency over a predetermined number of cycles.

The analog circuit of Figure 1 represents one prior art solution to the problem of sensing one of a plurality of input tone frequencies in the presence of noise as disclosed in GB-A-1482629. It may be referred to as a maximum likelihood quadrature tone detector for an unknown input phase. This prior art analog device suffers from lack of flexibility in that it must be designed for a single frequency and a predetermined bandwidth. It is also difficult to integrate a circuit of this type with other circuits of a using system.

Another prior art system which provides digital detection of incoming tones is described by A. D. Proudfoot, "Simple Multifrequency Tone Detector", *Electronics Letters*, October 19, 1972, Vol. 8, No. 21, Pp. 524-525. This system does not identify the phase of the incoming signal and it requires a complex digital reference signal for each incoming signal to be identified.

Summary of the invention

Solutions for these and other problems are provided for by the instant invention in a digital integrate and dump quadrature detector. The frequency to be detected is programmable and can be anywhere between the limits of direct current and one-half the sampling frequency, specified as accurately as necessary for use in a system. The system bandwidth is also programmable and is independent of the frequency of the incoming signal to be detected. The filter implementation is compatible with both integrated circuits and microprocessor realizations.

Therefore, it is an object of the invention to provide a digital decoder with a programmable reference frequency requiring minimum digital storage capacity.

It is another object of the invention to provide a programmable bandwidth characteristic which is independent of the incoming signal frequency.

It is still another object of the invention to provide phase identification of the incoming signal within any needed accuracy range.

It is yet another object of the invention to provide a tone detector circuit which is easily integrated with the using system.

According to the present invention there is provided apparatus for detecting at least one of a plurality of tones in an input signal from a signal source comprising:

programmable phase accumulator for generating a digital reference tone, said programmable accumulator providing a predetermined

number of output bits representing the instant phase of the digital reference tone;

decoder coupled to said programmable phase accumulator for accepting said predetermined number of output bits and for producing output code bits in response thereto;

input means coupled to the input signal source for filtering and digitizing the input signal, the digitized input signal having a positive phase and a negative phase;

a plurality of counters each coupled to said decoder and said input means, each of said counters being selected by a corresponding one of said output code bits, and each of said counters being responsive to a simultaneous combination of one of said output code bits and the digitized input signal from said input means; and

threshold detector means for determining when the absolute value of the difference between at least a first or a second predetermined pair of said plurality of counters is greater than a predetermined threshold and producing an output signal on at least one output terminal thereof for indicating the presence of said at least one of a plurality of tones when said predetermined threshold is exceeded.

These and other objects of the invention will be more readily understood after reading the detailed description which follows together with due consideration of the drawings.

Brief description of the drawings

Figure 1 illustrates, in block diagram form, a typical prior art system utilizing analog techniques.

Figure 2 represents a block diagram of a preferred embodiment of the invention.

Figure 3 illustrates an embodiment of the invention similar to that of Figure 2 wherein the limiter of Figure 2 is replaced by an A/D converter and the counters of Figure 2 are replaced by accumulators.

Figure 4 illustrates an implementation, in block diagram form, of weighted sine and cosine assignment for the Kth up/down counter or accumulator of Figure 2 or 3, and

Figure 5 shows, in block diagram form, an integrate-and-dump system wherein the timing is segmented into a plurality of portions. It may replace one of the counters of Figure 2.

Detailed description of the invention

A block diagram of digital tone detector 8 is shown in Figure 2. The detector consists of low-pass filter 10 and limiter 12 for operation on input signal 14, phase accumulator 16, 1 of 2ⁿ decoder 18, 2ⁿ up/down counters 20 (20a...20i), and threshold detector 22. (Figure 1 shows a prior art analog quadrature detector which may be used for comparison). Digital detector 8 operates by generating a digital local

reference which has the same frequency as the tone to be detected. The input signal is low-pass filtered, limited, and sampled. The sample, a 1 or -1, is then accumulated in one of 2^n counters 20 specified by the n most significant bits of the local reference phase at the sampling instant. The integrate-and-dump cycle consists of clearing all counters, accumulating a preset number of samples corresponding to a predetermined observation window, and then applying a threshold decision. In the following paragraphs, the local reference generator, decoder and counter operation, and threshold detector are discussed in detail.

Phase accumulator 16 comprises a multibit binary adder and register (not shown in detail) which are used to generate local reference signal 28. Output 24 of the adder is also connected to the register input; the output of the register is connected back to one of the inputs to the adder. The other input to the adder is programmable frequency input 26. For detecting a frequency f , programmable input 26 is set to the binary fraction corresponding to a ratio of f to f_s , the sampling frequency. This fraction f/f_s indicates the phase change that occurs in the local reference in the interval between sampling clock pulses. The fraction f/f_s is added to the accumulator at each sampling instant using modulo one arithmetic. Therefore, on overflow of the adder, the ones are dropped, leaving only the fractional part. The value in the accumulator represents a binary fraction between 0 and 1, corresponding to a phase angle of local reference 28 between 0° and 360° . The accumulator has m bits of precision, and therefore can specify the phase of the reference to 2^{-m} of a cycle. For $m=16$ and an 8 KHz sampling frequency, the corresponding frequency accuracy is 8000×2^{-16} or 0.122 Hz. Thus, for this case, the local reference can be any frequency between DC and 4 KHz, to the nearest 0.122 Hz.

The decoder and counters used in digital tone detector 8 correspond to multipliers 40 and integrators 42 of the quadrature detector (shown in Figure 1). 1 of 2^n decoder 18 uses the n most significant bits of phase accumulator 16 to divide one reference cycle into 2^n equal parts. Although n can be any number less than or equal to m , the total number of bits, only the $n=2$ case will be discussed here for simplicity. The implications of choosing larger values of n are discussed, infra.

There are four (2^n) up/down counters 20 (only two shown in Figure 2; 20a, 20i), one for each output of the 1-of-4 decoder. The output of decoder 18 indicates which of the four is to be counted after any sample clock; the output of limiter 12 indicates the direction of the count. A limiter 12 output "1" causes the selected counter to be incremented, while a "-1" causes it to be decremented. Each counter 20 is therefore accumulating the input samples for its quadrant of the reference cycle; first counter

20a accumulates the input signal when the reference phase is between 0 and .25, corresponding to 0° and 90° ; the second, .25 and .5, corresponding to 90° to 180° ; etc. In this way, if input signal 14 to detector 8 has the same frequency as local reference signal 28, the samples accumulated in each counter 20 will be in phase to within $\pm 45^\circ$, and the counts in accumulator 16 will increase in magnitude with continued sampling. If input signal 14 is not the same frequency as reference 28, or is noise, the samples in each counter 20 will not be in phase, and the samples will tend to cancel, causing the contents of the counters to remain near zero.

The operating cycle of detector 8 has three parts. First, counters 20 are reset by dump control timer 11. Next, samples are accumulated in counters 20, as described above. The number of samples accumulated determines the observation window, corresponding to integrate portions 42 of the integrate-and-dump quadrature detector (Figure 1). Finally, the threshold decision is applied to the accumulated samples in counters 20.

The threshold rule must examine all four counters 20, and determine whether or not input signal 14 was present during the observation window. The rule must be phase independent, since the phase of the detected signal may not match the reference. Labeling the accumulated samples in counters 20 as M_1 , M_2 , M_3 and M_4 , the detection rule is to compare the maximum of the magnitudes of $|M_1 - M_3|$ and $|M_2 - M_4|$ to a predetermined threshold T . That is, if the maximum of $|M_1 - M_3|$ or $|M_2 - M_4| > T$, the tone is present; otherwise it is absent.

Following is an operating example of tone detector 8 for a particular frequency and a discussion of the extraneous responses due to limiting and sampling and the effect of larger values of n , i.e.; more than four accumulating registers.

Assume a frequency f of 905 Hz is to be detected. The sampling frequency f_s is 8 KHz and the bandwidth of the detector is 30 Hz. From the previous discussion, the input to phase accumulator 16 must be the binary fraction given by f/f_s . This fraction is 0.11875, or in binary .0001 1110 0110 0110. This phase increment f/f_s is added to phase accumulator 16 at each sampling of input 26. In order to set the bandwidth the integrate-and-dump interval, controlled by timer 11, is chosen as 32 msec. (which is the reciprocal of the bandwidth), which corresponds to 256 samples of the input signal. These 256 samples are then accumulated in counters 20; each sample of the input is directed to its proper counter 20 by decoding the two most significant bits of phase accumulator 16. Since 256 samples are taken, approximately 64 will be directed to each counter 20. The exact number depends on the initial value of phase accumulator 16.

The integrate-and-dump cycle begins by

clearing all counters 20 with timer 11 and then accumulating 256 samples as described above. At the end of the sampling interval the criterion is calculated and the threshold test is applied. The criterion is the maximum of $|M_1 - M_2|$ or $|M_2 - M_4|$ where M_1 through M_4 represent the values in counters 20.

Extraneous responses arise due to the filtering and limiting of the input signal. Specifically, the response at $f/3$ is down by only 9.5 dB ($1/3$) and is due entirely to the hard-limiting of the original input signal. $f/5$, $f/7$, $f/9$, etc. responses also arise due to the limiter. A $3f$ term arises due to the effective hard-limiting of the local reference which comes about by using 4 counters to accumulate the input samples. There are $5f$, $7f$, $9f$, etc. responses due to the same limiting operation and their responses, due to sampling, are folded around the $f/2$ point. Other responses, such as $f/3$, $f/3$, arise due to a mixing action that occurs between the input sampling frequency and the harmonics of the input tone produced by the input limiter.

The detector discussed in the previous discussion is a quadrature integrate-and-dump detector using a limited input signal and a limited local reference. The extraneous signals are caused by these limiters. (Refer to Figure 3). Because of the inventive implementation of the quadrature detector the input limiter can be replaced by analog-to-digital (A/D) converter 50 without requiring two digital multiplications for each sample. In this case, the up/down counters of Figure 2 are replaced by accumulators 52, 54 and the digital value from A/D converter 50 is added to the selected accumulator corresponding to the current reference phase. The local reference limiting that is created by the four counter approach could be eliminated by using more than four counters. In particular, as the number of counters increases to 8, 16, etc., the harmonics of the local reference responses may be decreased to any arbitrary level. This may be accomplished by assigning to each accumulator or counter a sine and cosine value proportional to the sine and cosine value of its particular phase, as shown in Figure 4. The detection rule would be changed to multiply the contents of each accumulator by its corresponding sine and cosine values, and then emulate the square law detector as shown in Figure 1. The advantage of the system of Figure 4 over classical maximum likelihood detectors is that multiplication is performed only once at the end of each sample period rather than once for each input sample. Thus, the circuit may be modified if required to emulate the classical maximum likelihood integrate-and-dump quadrature detector.

This integrate-and-dump detector technique can be used to implement a pseudo-continuous detector for a system in which the start of the tone is unknown. An example of this implementation is shown in Figure 5. The sub-system of Figure 5 may be substituted for each of the counters 20 of Figure 2 to implement such a

pseudo-continuous detector. For example, using the previous example of an integration time of 32 milliseconds, this time can be broken into eight 4 millisecond integrate-and-dump segments. Counters 60 of Figure 6 are used to accumulate the segmented counts. Up/down control switch 64 and clock control switch 66 are controlled by a control signal (not shown) which is suitably synchronized with dump control timer 11 of Figure 2. The counter values for the last eight events may be summed together in adder 62. The proper threshold criteria may then be applied. This implementation leads to a detector with the same bandwidth as in the embodiment of the invention of Figure 2, but produces a detector output every 4 milliseconds rather than every 32 milliseconds.

In summary, an inventive implementation of a quadrature detector has been presented. It uses a more efficient detection algorithm than a classical detector or other digital filter detectors, and has the advantage of being fully programmable and easily implemented in a microprocessor or integrated circuit.

Various other modifications and changes may be made to the present invention from the principles of the invention as described above without departing from the scope thereof, as encompassed in the accompanying claims.

Claims

1. Apparatus for detecting at least one of a plurality of tones in an input signal from a signal source comprising:

programmable phase accumulator (e.g., Fig. 2; 16) for generating a digital reference tone, said programmable accumulator providing a predetermined number of output bits (e.g., 28) representing the instant phase of the digital reference tone;

decoder (e.g., Fig. 2; 18) coupled to said programmable phase accumulator for accepting said predetermined number of output bits and for producing output code bits in response thereto;

input means (e.g., Fig. 2; 10, 12) coupled to the input signal source for filtering and digitizing the input signal, the digitized input signal having a positive phase and a negative phase;

a plurality of counters (e.g., Fig. 2; 20a...20i) each coupled to said decoder and said input means, each of said counters being selected by a corresponding one of said output code bits, and each of said counters being responsive to a simultaneous combination of one of said output code bits and the digitized input signal from said input means; and

threshold detector means (22) for determining when the absolute value of the difference between at least a first or a second predetermined pair of said plurality of counters is greater than a predetermined threshold and producing an output signal on at least one output terminal thereof for indicating the presence

clearing all counters 20 with timer 11 and then accumulating 256 samples as described above. At the end of the sampling interval the criterion is calculated and the threshold test is applied. The criterion is the maximum of $|M_1 - M_2|$ or $|M_2 - M_4|$ where M_1 through M_4 represent the values in counters 20.

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In summary, an inventive implementation of a quadrature detector has been presented. It uses a more efficient detection algorithm than a classical detector or other digital filter detectors, and has the advantage of being fully programmable and easily implemented in a microprocessor or integrated circuit.

Various other modifications and changes may be made to the present invention from the principles of the invention as described above without departing from the scope thereof, as encompassed in the accompanying claims.

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1. Apparatus for detecting at least one of a plurality of tones in an input signal from a signal source comprising:

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decoder (e.g., Fig. 2; 18) coupled to said programmable phase accumulator for accepting said predetermined number of output bits and for producing output code bits in response thereto;

input means (e.g., Fig. 2; 10, 12) coupled to the input signal source for filtering and digitizing the input signal, the digitized input signal having a positive phase and a negative phase;

a plurality of counters (e.g., Fig. 2; 20a...20i) each coupled to said decoder and said input means, each of said counters being selected by a corresponding one of said output code bits, and each of said counters being responsive to a simultaneous combination of one of said output code bits and the digitized input signal from said input means; and

threshold detector means (22) for determining when the absolute value of the difference between at least a first or a second predetermined pair of said plurality of counters is greater than a predetermined threshold and producing an output signal on at least one output terminal thereof for indicating the presence



of said at least one of a plurality of tones when said predetermined threshold is exceeded.

2. The apparatus according to claim 1, modified in that a plurality of accumulators (e.g., Fig. 3, 52...54) are used in place of said plurality of counters.

3. Apparatus according to claim 1 further including circuit means (e.g., Fig. 4) for multiplying predetermined sine and cosine values with each output of said counters, and then squaring, summing and applying the result thereof to said threshold detector means.

4. The apparatus according to claim 1, wherein said counters comprise up/down counters (Fig. 2; 20a...20i), each of said up/down counters being responsive to a simultaneous combination of one of said output code bits and to a positive phase of the digitized input signal to count in an up direction, and being responsive to a simultaneous combination of one of said output code bits and to a negative phase of the digitized input signal to count in a down direction.

5. The apparatus according claim 1 wherein said input digitizing means comprises an analog to digital converter (e.g. Fig. 3; 50).

6. The apparatus according to claim 1 wherein each of said input digitizing means (e.g., Fig. 2; 12) comprises a limiter.

7. The apparatus according to claim 1 wherein each of said plurality of counters comprises a plurality of up/down counters (e.g., Fig. 5; 60a, 60b, 60n), each of said plurality of up/down counters being selected in a predetermined timed sequence by an up/down control switch (e.g., Fig. 5; 64, 66).

8. Apparatus according to any one of the preceding claims modified in that a microprocessor is used in place of and programmed to perform functions of programmable phase accumulator means, decoder, counters and threshold detector means.

Patentansprüche

1. Gerät zum Erfassen von wenigstens einem einer Vielzahl von Tönen in einem Eingangssignal von einer Signalquelle, mit folgenden Merkmalen:

einem programmierbaren Phasensammler (z.B. Fig. 2; 16) zum Erzeugen eines digitalen Bezugstones, wobei der programmierbare Sammler eine vorbestimmte Anzahl von Ausgangs-Bits (z.B. 28) vorsieht, die die momentane Phase des digitalen Bezugstones darstellen;

einem Decoder (z.B. Fig. 2; 18), der an den programmierbaren Phasensammler angeschlossen ist, um die vorbestimmte Anzahl von Ausgangs-Bits aufzunehmen und um in Antwort hierauf Ausgangscode-Bits zu erzeugen;

einer Eingangseinrichtung (z.B. Fig. 2; 10, 12), die an die Eingangssignalquelle zum Filtern und Digitalisieren des Eingangssignales angeschlossen ist, wobei die digitalen Eingangs-

signale eine positive Phase und eine negative Phase haben;

eine Vielzahl von Zählern (z.B. Fig. 2; 20a...20i), die jeweils an den Decoder und an die Eingangseinrichtung angeschlossen sind, wobei jeder der Zähler durch ein entsprechendes der Ausgangscode-Bits ausgewählt wird, und wobei jeder der Zähler auf eine gleichzeitige Kombination von einem der Ausgangscode-Bits und dem digitalisierten Eingangssignal von der Eingangssignaleinrichtung anspricht; und

einer Schwellenwert-Detektoreinrichtung (22), um zu bestimmen, ob der absolute Wert der Differenz zwischen wenigstens einem ersten und einem zweiten vorbestimmten Paar der Vielzahl von Zählern größer ist als eine vorbestimmte Schwelle, und um ein Ausgangssignal an wenigstens einem von dessen Ausgangsklemmen zu erzeugen, um das Vorliegen von dem wenigstens einen der Vielzahl von Tönen anzuzeigen, wenn die vorbestimmte Schwelle überschritten ist.

2. Gerät nach Anspruch 1, das darin abgeändert ist, daß eine Vielzahl von Sammlern (z.B. Fig. 3, 52...54) anstelle der Vielzahl von Zählern benutzt wird.

3. Gerät nach Anspruch 1, ferner mit einer Schaltungseinrichtung (z.B. Fig. 4) zum Multiplizieren vorbestimmter Sinus- und Kosinuswerte mit jedem Ausgang der Zähler, und zum Quadrieren, Summieren und Zuführen des Ergebnisses hiervon zu der Schwellenwert-Detektoreinrichtung.

4. Gerät nach Anspruch 1, bei dem die Zähler Aufwärts-/Abwärts-Zähler (Fig. 2; 20a...20i) enthalten; wobei jeder der Aufwärts-/Abwärts-Zähler auf die gleichzeitige Kombination von einem der Ausgangscode-Bits und auf eine positive Phase der digitalisierten Eingangssignale anspricht, um in eine Aufwärtsrichtung zu zählen, und auf die gleichzeitige Kombination von einem Ausgangscode-Bits und auf die negative Phase des digitalisierten Eingangssignals anspricht, um in eine Abwärtsrichtung zu zählen.

5. Gerät nach Anspruch 1, bei dem die Eingangs-Digitalisierungseinrichtung einen Analog-zu-Digital-Wandler (z.B. Fig. 3; 50) aufweist.

6. Gerät nach Anspruch 1, bei dem jede der Eingangs-Digitalisierungseinrichtungen (z.B. Fig. 2; 12) einem Begrenzer aufweist.

7. Gerät nach Anspruch 1, bei dem jeder der Vielzahl von Zählern eine Vielzahl von Aufwärts-/Abwärts-Zählern (z.B. Fig. 5; 60a, 60b, 60n) hat, wobei jeder der Vielzahl von Aufwärts-/Abwärts-Zählern in einer vorbestimmten Zeitreihenfolge durch einen Aufwärts-/Abwärts-Steuerschalter (z.B. Fig. 5; 64, 66) ausgewählt wird.

8. Gerät nach einem der vorhergehenden Ansprüche, das darin verändert ist, daß ein Mikroprozessor anstelle der programmierbaren Phasenswandlereinrichtung, des Decoders, der Zähler und der Schwellenwert-Detektorein-



richtung verwendet wird und dazu programmiert ist, um die Funktionen der programmierbaren Phasensammleineinrichtung, des Decoders, der Zähler und der Schwellenwert-Detektoreinrichtung auszuführen.

Revendications

1. Appareil permettant de détecter au moins l'une de plusieurs audiofréquences dans un signal d'entrée venant d'une source de signaux, comprenant:

un accumulateur de phase programmable (par exemple figure 2; 16) destiné à produire une audiofréquence de référence numérique, ledit accumulateur programmable fournissant un nombre prédéterminé de bits de sortie (par exemple 28) qui représentent la phase instantanée de l'audiofréquence de référence numérique;

un décodeur (par exemple figure 2; 18) couplé audit accumulateur de phase programmable afin de recevoir ledit nombre prédéterminé de bits de sortie et de produire des bits de code de sortie en réponse à ceux-ci;

un moyen d'entrée (par exemple figure 2; 10, 12) couplé à la source de signaux d'entrée afin de filtrer et de mettre sous forme numérique le signal d'entrée, le signal d'entrée mis sous forme numérique ayant une phase positive et une phase négative;

plusieurs compteurs (par exemple figure 2; 20a,...,20i) qui sont chacun couplés audit décodeur et audit moyen d'entrée, chacun desdits compteurs étant sélectionnés par l'un correspondant desdits bits de code de sortie, et chacun desdits compteurs répondant à une combinaison simultanée de l'un desdits bits de code de sortie et du signal d'entrée mis sous forme numérique venant dudit moyen d'entrée; et

un détecteur de seuil (22) servant à déterminer si la valeur absolue de la différence entre les éléments d'au moins une première ou une deuxième paire prédéterminée desdits compteurs est supérieure à un seuil prédéterminé et à produire un signal de sortie sur au moins l'une de ses bornes de sortie afin d'indiquer la présence de ladite audiofréquence prise parmi

plusieurs audiofréquences lorsque ledit seuil prédéterminé est dépassé.

2. Appareil selon la revendication 1, modifié en ce que plusieurs accumulateurs (par exemple figure 3; 52,...,54) sont utilisés à la place des compteurs.

3. Appareil selon la revendication 1, comportant en outre un circuit (par exemple figure 4) servant à multiplier des valeurs de sinus et cosinus prédéterminées avec chaque signal de sortie desdits compteurs, et à ensuite élever au carré, additionner et appliquer le résultat audit détecteur de seuil.

4. Appareil selon la revendication 1, où lesdits compteurs comprennent des compteurs ascendants-descendants (par exemple figure 2; 20a,...,20i), chacun desdits compteurs ascendants-descendants répondant à une combinaison simultanée de l'un desdits bits de code de sortie et à une phase positive dudit signal d'entrée mis sous forme numérique en comptant dans le sens ascendant, et répondant à une combinaison simultanée de l'un desdits bits de code de sortie et à une phase négative du signal d'entrée mis sous forme numérique en comptant dans le sens descendant.

5. Appareil selon la revendication 1, où ledit moyen de mise sous forme numérique d'entrée comprend un convertisseur analogique-numérique (par exemple figure 3; 50).

6. Appareil selon la revendication 1, où chacun desdits moyens de mise sous forme numérique d'entrée (par exemple figure 2; 12) comprend un limiteur.

7. Appareil selon la revendication 1, où chacun desdits compteurs comprend plusieurs compteurs ascendants-descendants (par exemple figure 5; 60a, 60b, 60n), chacun desdits compteurs ascendants-descendants étant sélectionné suivant une séquence cadencée prédéterminée par un commutateur de commande ascendant-descendant (par exemple figure 5; 64, 66).

8. Appareil selon l'une quelconque des précédentes revendications modifié en ce qu'un microprocesseur est utilisé à la place de l'accumulateur de phase programmable, du décodeur, des compteurs et du détecteur de seuil et est programmé pour effectuer leurs fonctions.

