A ROBUST DEVICE CARRIER FOR FORMING A SEMICONDUCTOR PACKAGE

Field Of Invention

The present invention generally relates to packaging of a semiconductor device. More particularly, the invention relates to a device carrier for packaging of the semiconductor device.

Background

In the past, the semiconductor industry has seen integrated circuits (IC) being produced with fewer IC pads and interconnect structures. This has enabled the spacing apart of the leads and interconnect structures in the IC. However recent IC packages have become more compact and requires increased functions to be incorporated into a die. Additionally, the die has to be dimensionally small to enable the IC packages to compact. It is therefore desirable for the interconnect structures to be kept spaced apart while increasing the number of interconnects due to the increased logic on the die. The increased logic translates into an increase in circuit density of the die. As circuit density increases on progressively smaller dies, it becomes important to provide a thin, reliable and robust packaging for forming the miniature packages. Also, the mechanical, electrical and heat dissipation properties of such miniature packages needs to be carefully considered without affecting the overall performance of the said IC.

Furthermore, a general concern for an IC package during IC packaging of a semiconductor device is on the integrity of the IC package structure. The IC package structure typically comprises a substrate with the semiconductor device coupled to the substrate. Typically the substrate may be damaged due to, for example, cracks in the substrate when the substrate is subjected to stress. The substrate may be stressed during, for example, coupling of the semiconductor device to the substrate or handling of the IC package.

Additionally, after coupling the semiconductor device to the substrate, the structure of the IC package may also be weakened due to additional stress on the substrate and hence renders the IC package more susceptible to damages. Damages in the substrate adversely affect the integrity of the IC package structure. Conventional implementations to improve the integrity of the IC package structure include improving robustness of the IC package structure via an underfill process. The typical underfill process comprises providing insulation materials within the IC. The insulation material may serve to support the semiconductor device to reduce stress in the substrate. However, distribution of the insulation material within the IC package may be inconsistent, particularly, between the semiconductor device and the substrate. The inconsistent distribution may lead to low volume compactness of the support for the semiconductor device. Consequently the support which the insulation material provides in the IC may be limited.

It is therefore desirable to provide a solution to address at least one of the foregoing problems of the conventional operations.

Brief Description Of The Drawings

The invention is described hereinafter with reference to the following drawings, in which:

FIGs. 1a-g show a device carrier for packaging a semiconductor chip in accordance with an embodiment of the invention;

FIG. 2 shows an assembly comprising the device carrier of Fig. 1a;

FIGs. 3a-b show a device package formed from the assembly of Fig. 2;

FIGs. 4a-b show a carrier array formed using a plurality of the device carrier of Fig. 1a being formed as part of a carrier array;

FIG 5 shows a process flow chart of a method for forming the device carrier of Fig. 1a; and

FIG 6 shows a process flow chart of a method for forming the device package of Fig. 4a.

Detailed Description

For purposes of brevity and clarity, the description of the present invention is limited hereinafter to a method and a device carrier for packaging a semiconductor device. This however does not preclude various embodiments of the invention from other applications where fundamental principles prevalent among the various embodiments of the invention such as operational, functional or performance characteristics are required.

An exemplary embodiment of the invention, a device carrier 100 for packaging a semiconductor device for addressing the foregoing problems of conventional semiconductor device packaging structures, is described hereinafter with reference to Figs. 1-3. Figs 1a, 1b, 1e and 1f provide cross section side views of the device carrier 100 and Figs 1c, 1d and 1g provide top views of the device carrier 100. The device carrier 100 comprises a device substrate 110 and a stiffener structure 120 as shown in Fig. 1a. Fig. 1a is a sectional elevation of the device carrier 100 according to view A-A of Fig. 1c. The device substrate 110 comprises one or more insulating portions 114 and one or more conductive portions 118. The device substrate 110 is, for example, a molded substrate and has a first face 110a and a second face 110b. The first face 110a outwardly opposes the second face 110b. Each of the one or more insulating portion 114 is preferably formed from insulation materials such as dielectric material or mold material. Each of the one or more conductive portions 118 comprises one or more conductive traces 118a and one or more studs 118b quantitatively corresponding with the conductive traces 118a. The conductive traces 118a extend toward the first face 110a, away from the second face 110b. The studs 118b extend from the conductive traces 118a, towards the first face 110a. Preferably at least one of the one or more studs 118b extends from each of the conductive traces

118a. The one or more studs 118b preferably correspond to contact pad configuration of footprints of a peripheral device (not shown). The peripheral device is, for example, a printed circuit board (PCB) with the contact pad being an array of solder pads on the PCB. The device carrier 100 is couplable to the PCB by, for example, soldering the studs 118b to the solder pads on the PCB. Preferably, each of the one or more conductive portions 118 defines an array segment 119a in the carrier structure 110 as shown in Fig 1c. Preferably, periphery 119b of each of the array segment circumscribes each of the conductive portions 118.

The stiffener structure 120 extends from the second face 110b and is preferably formed from a material such as a polymer or a metal. Alternatively, the stiffener structure 120 is formed from a combination of two or more materials as shown in Fig. 1b. Each of the combination of two or more materials forms multiple material layers, for example, a first material layer 125a and a second material layer 125b. The different materials include for example polymers and metals. For example, the first material layer 125a comprises polymers and the second material layer 125b comprises metals. Preferably, the stiffener structure 120 extends away from opposing edges of the periphery 119b of each array segment 119a to define a cavity 130 as illustrated in Fig. 1c. In other words, the stiffener structure is preferably disposed away from the array segment 119a. Preferably the stiffener structure 120 is a ring structure. Preferably, the ring structure is a continuous ring joint. The continuous ring joint comprises a single ring shaped section 120' extending adjacently along the periphery of the device substrate 110 as shown in Fig. 1c. Alternatively, the ring structure is a discontinuous ring joint. The discontinuous ring joint comprises a plurality of discontinuous sections 128a- 128d substantially extending along the periphery of the device substrate 110 as shown in Fig. 1d. Preferably, the ring structure has a substantially primitive geometric shape. Examples of the substantially primitive geometric shape are shapes such as a rectangular, a square or a circle. Alternatively, the ring structure has an irregular shape.

The stiffener structure 120 preferably comprises one or more locking portions 170 as shown in Fig. 1e. The locking portions 170 preferably extend towards the first face

110a of the device substrate 110 from the second face 110b of the device substrate 110. The locking portions 170 are integrated with the stiffener structure 120. Alternatively, the locking portions 170 are electroplated to the stiffener structure. The locking portions 170, preferably, provide locking structures for substantially anchoring the stiffener structure 120 to the carrier structure 110 to improve robustness of the device carrier 100. Alternatively, the stiffener structure 120 is connected to at least one of the one or more conductive portions via at least one of the one or more conductive traces 118a as shown in Fig. 1f. Fig 1f is a sectional elevation of the device carrier 100 according to view B-B of Fig. 1g. Preferably, when the stiffener structure is connected to at least one of the one or more conductive traces 118a, the locking portions 170 extend from the stiffener structure 120 towards the first face 110a of the device substrate 110 for coupling with the peripheral device.

The device carrier 100 is preferably used to package one or more semiconductor devices to form an assembly 200 as shown in Fig. 2. An example of a semiconductor device is a semiconductor chip 205 such as a memory chip. The semiconductor chip 205 preferably has a first face 205a and a second face 205b. The second face 205b outwardly opposes the first face 205a. Alternatively, the device carrier 100 is used to package integrated circuit (IC) chips. The semiconductor chip 205 comprises one or more terminals, for example, a first terminal 210 and a second terminal 220. Preferably, the first and second terminals 210/220 are formed on the second face 205b of the semiconductor chip 205. The first and second terminals 210/220 are contacts of the semiconductor chip 205. For example, the first and second terminals 210/220 are, respectively, the voltage supply and ground contacts of a memory chip. Preferably, the semiconductor chip 205 is substantially disposed within the cavity 130 of the device carrier 100. Alternatively, at least a portion of the semiconductor chip 205 is disposed within the cavity 130 of the device carrier 100. The assembly 200 comprises an interconnect structure 240. The interconnect structure 240 is provided within the cavity 130 to couple the semiconductor chip 205, via the first and second terminals 210/220, to the device substrate 110. Preferably, electrical signals are communicable between the studs 118b and at least one of the first and second terminal 210/220 of the semiconductor chip 205 via the interconnect structure 240.

The interconnect structure 240 comprises one or more electrical interconnect paths, for example a first interconnect path and a second interconnect path. Each of the first and second interconnect paths comprises at least one of a first interconnect layer 240a and a second interconnect layer 240b. The first interconnect layer 240a is preferably formed from a conductive material such as copper. The second interconnect layer 240b is preferably formed from a solder material such lead or tin. Examples of the electrical interconnect paths are pillar bumps and solder bumps. Each of the one or more conductive portions 118 is preferably conductive redistribution paths extending between the first and second faces 110a/b of the device substrate 110.

Preferably the assembly 200 is injected with an underfill to form a device package 300 as shown in Fig. 3a. The underfill is disposed within the device package 300 and comprises at least one of a first filling material 250a and a second filling material 250b. The first filling material 250a is preferably a first insulative material or a first dielectric material. The second filling material 250b is preferably a second insulative material or a second dielectric material. The underfill, preferably, substantially fills empty areas within the device package 300. For example, the first filling material 250a is substantially disposed between the second face 110b of the device substrate 110 and the second face 205b of the semiconductor chip 205 to fill the empty areas between the second face 110b of the device substrate 110 and the second face 205b of the semiconductor chip 205. The second filling material 250b is, preferably, disposed substantially between the stiffener structure 120 and the semiconductor chip 205 to fill empty areas between the stiffener structure 120 and the semiconductor chip 205. As can be readily appreciated, the cavity 130 defined by the stiffener structure 120 facilitates a substantially high volume compactness of the underfill within the device package 300. Furthermore, the stiffener structure 120 provides additional support for the device substrate 110 in the device package 300 by, for example, impeding flexure of the device substrate 110.

The device package 300 further comprises a seal structure 310 as shown in Fig. 3b. The seal structure 310 is preferably disposed over the semiconductor chip 205 and couples with the stiffener structure 120 to substantially enclose the semiconductor

chip 205 within the cavity 130. The seal structure 310 is preferably formed from metals and is used for applications such as electromagnetic shielding or heatsinking. When used as a heatsink, the seal structure 310 preferably contacts the semiconductor chip 205 to conduct heat dissipated from the semiconductor chip 205. Alternatively, a heat conductive layer 320 is disposed between the seal structure 310 and semiconductor chip 205 to thermal communicate the heat conductive layer with the seal structure 310 to conduct heat dissipated from the semiconductor chip 205.

Preferably, a plurality of each of the one or more conductive portions 118 forms a carrier array 400 as shown in Fig. 4a- 4b. The carrier array 400 is, for example, a one by two array as shown in Fig. 4a. Fig. 4b provides a top view of the one by two array The one by two array comprises a plurality of the device carrier 100, for example a first device carrier 100a and a second device carrier 100b. Each of the first and second carrier device 100a/b comprises the stiffener structure 120. A singulation portion 410 is formed between the stiffener structure 120 of the first carrier device 100a and the stiffener structure 120 of the second carrier device 100b. The singulation portion 410 facilitates separation of the first and second carrier device 100a/b and substantially preserves integrity of each of the first and second device carrier 100a/b by impeding flexure to each of the first and second device carrier 110a/b.

The device carrier 100 is preferably formed using a method 500 as shown in Fig. 5. The method 500 comprises providing a sacrificial layer and forming patterned traces on a sacrificial layer at step 510. Preferably, the patterned traces comprise a first trace layer and a second trace layer. Preferably, the first trace layer corresponds to at least one of the conductive traces 118a and the locking portions 170 and the second trace layer corresponds to the studs 118b. Preferably, the patterned traces are formed on the sacrificial layer via electroplating. For example, the first trace layer is electroplated onto the sacrificial layer and the second trace layer is electroplated to the first trace layer thereafter. The sacrificial layer is preferably a conductive layer. Preferably, the conductive layer is a metal strip such as copper. Following this, an insulating layer is deposited over the patterned traces at step 520. Preferably, the

insulating layer is a mold material and the patterned traces are molded in the mold material to form an over-mold layer. Preferably, the patterned traces define at least one of the one or more conductive portions 118 and the locking portions 170. Preferably, the over-mold layer forms an excess layer over the conductive portions. The one or more stiffener structures 120 is preferably formed by further patterning the sacrificial layer The sacrificial layer is preferably further patterned by, for example, conventional etch and mask techniques such as window etching. In other words, a portion of the sacrificial layer is removed to form the stiffener structure 120. Alternatively, the sacrificial layer is removed by, for example, etching and the stiffener structure 120 is formed from an insulating material. As described above, the patterned traces are formed on the sacrificial layer via electroplating. It can be readily appreciated that other conventional techniques such as mask and etch techniques are also usable for forming the patterned traces, for example etching the sacrificial layer to form the patterned traces. The method 500 further comprises the step of material removal. Examples of material removal are grinding the over-mold layer to at least reduce the excess layer. Preferably, the excess layer is removed to form the device substrate 110 of the device carrier 100.

The device package 300 is preferably formed using a method 600 as shown in Fig. 6. The method 600 comprises forming the device carrier 100 at step 610 and coupling the semiconductor chip 205 to the device carrier 100 at step 620. The device carrier 100 is preferably formed using the method 500 as shown in Fig. 5. The semiconductor chip 205 is preferably attached to the device carrier 100 via the interconnect structure 240. Following this, at step 630, the assembly 200 is injected with the underfill to form device package 300.

In the foregoing manner, a device carrier for packaging a semiconductor device and method for forming the device carrier are described for addressing at least one of the foregoing disadvantages. The invention is not to be limited to specific forms or arrangements of parts so described and it will be apparent to one skilled in the art in view of this disclosure that numerous changes and/or modification can be made without departing from the scope and spirit of the invention.