"System for the rapid transmission of messages between computers".

The present invention relates to a system for the rapid transmission of messages between computers connected to a single bus to which there is also connected a main memory.

This type of network is known wherein the transmission of a message from one computer to another is obtained with the aid of a writing cycle in the main memory effected by the emitter computer followed by a main memory reading cycle effected by the receiving computer. Accordingly, a device for the time-division of the access to the main memory has to be provided in order to prevent any interference between the information circulating on the bus. The computers are all provided with a private memory permitting them to locally effect the majority of required operations, and one of them, known as the central computer, carries out administration of the system, i.e. the control of the various elements of the network.

Since in this type of system, the private memory of each of the computers becomes more and more important, the messages transferred by means of the bus become longer and longer. As a result traffic saturation occurs on the bus and access difficulties occur between the computers and the main memory.

It is an object of the present invention to avoid, on transmission of messages in between two computers, utilization of the bus which firstly helps to reduce the saturation of the bus and secondly reduces the time necessary for transmission since the successive writing and reading cycles in the dialogue of a computer with a further computer through the intermediary of the main memory are suppressed.

According to the present invention there is provided a system for the rapid transmission of messages between computers including a central computer controlling the operation of the system, all the computers being connected to a single bus to which is also connected a main memory, each of the computers being provided with a private memory, said system including an electronic switch to which the computers are connected, the electronic switch being controlled by the central computer through the intermediary of the bus in such a manner that said electronic switch interconnects the computers and enables the messages of all length to be directly transmitted between said computers, the bus being only used to enable the computers to have access to the main memory.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawing, wherein the sole figure is a block diagram of a preferred form of a system for the rapid transmission of messages.

With reference to the drawing, the computer controlling the operation of the system is a central computer 1. The central computer 1 comprises a private ———————

memory 2 and also a time-division device 3 for access to a main memory 6 including a scrutiny circuit permitting detecting the peripheral computer, having demanded via the bidirectional connection 4 being connected to the bus 5 so as to have access to the main memory 6, and a decision circuit supplying the authorization to the computer which has demanded access as soon as the latter is free.

In the system illustrated, only three peripheral computers 7, 8 and 9, each having respective private memories 10, 11 and 12 have been shown, but it will be obvious that the number of peripheral computers associated with the system may differ from three. In a preferred form, the main memory 6 has the capacity of 512 k words of 16 binary elements, whereas the private memories 2, 10, 11 and 12 each have a capacity of 256 k words.

In order to prevent the messages exchanged between two computers from circulating via the bus 5 and the main memory 6, so as to reduce the traffic on the bus 5 whilst at the same time increasing the speed of transmission of the messages, an electronic switch 13 is connected to each of the computers.

The electronic switch 13 is a telephonic auto-switch which is capable of providing without blocking the switching of sixteen numerical connections having a velocity of 8 Mtit/s.

The electronic switch 13 is also controlled by the central computer 1 through the intermediary of the bus 5.

When a peripheral computer, for example, the

computer 9, requests the sending of a message to the attention of a further computer, for example the peripheral computer 7, it addresses its request to the central computer 1 through intermediary of the bidirectional connection 4. Since the computer 9 does not request access to the main memory 6, the message may be directly dispatched to the computer 7 through the intermediary of the electronic switch 13. The electronic switch then receives, through the intermediary of the bus 5, the order to connect the two computers 9 and 7, unless the requested computer is already occupied.

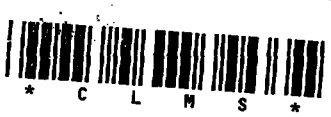
Consequently, a plurality of inter-computer connections may be simultaneously established and as a result there is a very substantial increase in the speed of the transmission of messages between peripheral computers. Furthermore, the bus 5 and the main memory are freed from their respective functioning of message transfer and may thus be utilized for other purposes.

In the example considered above, there are normally required 3.5 µs for transferring a word of 16 binary elements from a computer to the main memory and then 3.5 µs for transferring the same word from the main memory to a second computer, and knowing that the central computer 1 occupies the bus 5 during half the time, the total time required for the transfer of one word of a computer to another is equal to 14 µs. In the above described system, the transfer is effected only 2 µs,

i.e. 7 times more rapidly.

Furthermore, the waiting is substantially reduced since a plurality of simultaneous connections may be carried into effect. However, an additional inlet-output interface circuit may be provided for this purpose in each of the computers, all the more since transmission may be effected according to the synchronous mode.

In a modified form, according to the selected interface circuit, the switch 13 may equally well be of a special type and of the time-type.



CLAIMS:

1. A system for the rapid transmission of messages between computers including a central computer controlling the operation of the system, all the computers being connected to a single bus to which is also connected a main memory, each of the computers being provided with a private memory said system including an electronic switch to which the computers are connected, the electronic switch being controlled by the central computer through the intermediary of the bus in such manner that said electronic switch interconnects the computers and enables the messages of all length to be directly transmitted between said computers, the bus being only used to enable the computers to have access to the main memory.

2. A system according to Claim 1, wherein the electronic switch is a telephonic auto-switch.

3. A system for the ripid transmission of messages between computers constructed and arranged to operate substantially as herein described with reference to the accompanying drawing.