**CLAIMS**

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a water-soluble matrix based on a solid component and water, and the mask comprising a p-block metal compound, an s-block metal compound, or a transition metal compound dissolved throughout the water-soluble matrix;

patterning the mask and a portion of the semiconductor wafer with a laser scribing process to provide a patterned mask with gaps and corresponding trenches in the semiconductor wafer in regions between the integrated circuits; and

plasma etching the semiconductor wafer through the gaps in the patterned mask to extend the trenches and to singulate the integrated circuits, wherein the patterned mask protects the integrated circuits during the plasma etching.

2. The method of claim 1, wherein plasma etching the semiconductor wafer comprises using a fluorine-based etch chemistry, and the p-block metal compound, the s-block metal compound, or the transition metal compound is resistant to the fluorine-based etch chemistry.

3. The method of claim 1, wherein the p-block metal compound comprises an aluminum cation or a tin cation, or wherein the s-block metal compound comprises a potassium cation or a calcium cation, or wherein the transition metal compound comprises a copper cation, a nickel cation, a silver cation, or a chromium cation.

4. The method of claim 1, wherein the p-block metal compound, the s-block metal compound, or the transition metal compound comprises an acetate anion.

5. The method of claim 1, wherein the solid component of the water-soluble matrix is poly(vinyl alcohol) (PVA), and wherein the water-soluble matrix further comprises poly(vinyl pyrrolidone).

6. The method of claim 1, wherein plasma etching the semiconductor wafer comprises plasma etching a single crystalline silicon wafer, and wherein a ratio of an etch rate of the single crystalline silicon wafer to an etch rate of the mask is approximately in the range of 36:1 – 140:1 during the plasma etching.

7. The method of claim 1, further comprising:

prior to forming the mask above the semiconductor wafer, performing a plasma or chemical pre-treatment on the semiconductor wafer to increase wettability and coating of the mask on the semiconductor wafer.

8. The method of claim 1, further comprising:

subsequent to plasma etching the semiconductor wafer, removing the patterned mask using an aqueous solution.

9. The method of claim 1, further comprising:

subsequent to patterning the mask and prior to plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits, cleaning the trenches in the semiconductor wafer with a plasma cleaning process.

10. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a water-soluble matrix based on a solid component and water, and the mask comprising a p-block metal compound, an s-block metal compound, or a transition metal compound dissolved throughout the water-soluble matrix; and

patterning the mask and singulating the integrated circuits of the semiconductor wafer with a plasma etching process, wherein the patterned mask protects the integrated circuits during the plasma etching.

11. The method of claim 10, wherein the p-block metal compound comprises an aluminum cation or a tin cation, or wherein the s-block metal compound comprises a potassium cation or a calcium cation, or wherein the transition metal compound comprises a copper cation, a nickel cation, a silver cation, or a chromium cation, and wherein the p-block metal compound, the s-block metal compound, or the transition metal compound comprises an acetate anion.

12. The method of claim 10, wherein the solid component of the water-soluble matrix is poly(vinyl alcohol) (PVA), and wherein the water-soluble matrix further comprises poly(vinyl pyrrolidone).

13. The method of claim 10, wherein forming the mask above the semiconductor wafer comprises spin-coating the mask on the semiconductor wafer.

14. The method of claim 10, further comprising:

subsequent to patterning the mask and singulating the integrated circuits of the semiconductor wafer with the laser scribing process, removing the patterned mask using an aqueous solution.