

THIS SHEET HAS BEEN
REPLACED

ABSTRACT

PROTECTION SYSTEM FOR CRITICAL MEMORY INFORMATION

5 A computer system, typically a postage meter system,
has a processor (10), a memory (11, 12, 13), an address
decoder (16), and a window circuit (70). The window
circuit selectively couples the write strobe output (15)
10 of the processor with the write strobe input of the
memory in response to the processor's setting and
clearing of a latched signal. A counter resets the
processor if the latched signal is set and not cleared
within a predetermined time period.

This Sheet Has Been Replaced

