What is claimed : ~~CLAIMS~~

1. A computing system comprising:

a housing, wherein a lower pressure is maintained inside the housing than an atmospheric pressure outside the housing; a first plurality of components; a second plurality of components;

a first substrate, inside the housing, arranged in a first plane having a first surface and a second surface parallel to the first plane, wherein the second surface is opposite to the first surface, wherein a first set of the first plurality of components is attached to the second surface towards a first end of the first substrate and wherein a second set of the second plurality of components is attached to the second surface towards a second end of the first substrate, wherein the first end is opposite to the second end, wherein each of the first plurality of components is configured to provide primarily a processor functionality and wherein each of the second plurality of components is configured to provide primarily a storage functionality;

a second substrate, inside the housing, arranged in a second plane above or below the first plane, the second substrate having a third surface and a fourth surface parallel to the second plane, wherein the fourth surface is opposite to the third surface, wherein a third set of the first plurality of components is attached to the fourth surface towards a third end of the second substrate and wherein a fourth set of the second plurality of components is attached to the fourth surface towards a fourth end of the second substrate, wherein the third end is opposite to the fourth end, and wherein each of the first substrate and the second substrate comprising a plurality of circuit traces for interconnecting at least a subset of the first plurality of the components with at least a subset of the second plurality of components; and

a heat-shield configured to thermally separate the first end from the second end of the first substrate and thermally separate the third end from the fourth end of the second substrate such that each of the first plurality of components is configured to operate at a first temperature and each of the second plurality of components is configured to operate at a second temperature greater than the first temperature, and wherein the first temperature is in a range between 2 Kelvin to 77 Kelvin and wherein

the second temperature is in a range between 200 Kelvin to 400 Kelvin.

2. The computing system of claim 1, wherein the lower pressure is in a range between 10^{3} Torr to 10^{10} Torr.

3. The computing system of claim 1, wherein the primary processor functionality comprises at least one of a central-processing functionality, a graphics-processing functionality, an artificial-intelligence functionality, a gate-array functionality, a memory functionality, or a bus-interface-management functionality.

4. The computing system of claim 1, wherein the primary storage functionality comprises at least one of a memory functionality, gate-array functionality, a bus-management functionality, a controller functionality, or a bus-interface-management functionality.

5. The computing system of claim 1, wherein each of the first plurality of components is selected from a group comprising a central processing unit, a graphics-processing unit, an artificial-intelligence processor, a field-programmable gate array, an application-specific integrated circuit, an application-specific standard product, a system-on-a-chip, a complex programmable logic device, a random-access memory, and a Josephson magnetic random-access memory.

6. The computing system of claim 1, wherein each of the second plurality of components is selected from a group comprising a dynamic random-access memory, a field-programmable gate array, an application-specific integrated circuit, an application-specific standard product, a system-on-a-chip, and a complex programmable logic device.

7. The computing system of claim 1, wherein in each of the plurality of circuits traces comprises a first region including a superconducting metal but excluding a normal metal and a second region including both the superconducting metal and the normal metal.

8. A computing system comprising:
a housing, wherein a vacuum is maintained inside the housing; a first plurality of components; a second plurality of components
a first substrate, inside the housing, arranged in a first plane having a first surface and a second surface parallel to the first plane, wherein the second surface is opposite to the first surface, wherein a first set of the

first plurality of components is attached to the second surface towards a first end of the first substrate and wherein a second set of the second plurality of components is attached to the second surface towards a second end of the first substrate, wherein the first end is opposite to the second end, wherein each of the first plurality of components is configured to provide primarily a processor functionality and wherein each of the second plurality of components is configured to provide primarily a storage functionality, ~~and wherein a first heat sink is coupled to the first substrate to thermally clamp the first substrate;~~

a second substrate, inside the housing, arranged in a second plane above or below the first plane, the second substrate having a third surface and a fourth surface parallel to the second plane, wherein the fourth surface is opposite to the third surface, wherein a third set of the first plurality of components is attached to the fourth surface towards a third end of the second substrate and wherein a fourth set of the second plurality of components is attached to the fourth surface towards a fourth end of the second substrate, wherein the third end is opposite to the fourth end, and wherein each of the first substrate and the second substrate comprising a plurality of circuit traces for interconnecting at least a subset of the first plurality of the components with at least a subset of the second plurality of components, and ~~wherein a second heat sink is coupled to the second substrate to thermally clamp the second substrate; and~~

a heat-shield configured to thermally separate the first end from the second end of the first substrate and thermally separate the third end from the fourth end of the second substrate such that each of the first plurality of components is configured to operate at a first temperature and each of the second plurality of components is configured to operate at a second temperature greater than the first temperature, and wherein the first temperature ~~is below 9 Kelvin and wherein the second temperature~~ is in a range between 2 Kelvin to 77 Kelvin and wherein the second temperature is in a range between 200~~80~~ Kelvin to 400 Kelvin.

9. The computing system of claim 8, wherein the vacuum corresponds to a pressure in a range between 10^{3} Torr to 10^{10} Torr.

10. The computing system of claim 8, wherein the primary processor functionality comprises at least one of a central-processing functionality, a graphics-

processing functionality, an artificial-intelligence functionality, a gate-array functionality, a memory functionality, or a bus-interface-management functionality.

11. The computing system of claim 8, wherein the primary storage functionality comprises at least one of a memory functionality, gate-array functionality, a bus-management functionality, a controller functionality, or a bus-interface-management functionality.

12. The computing system of claim 8, wherein each of the first plurality of components is selected from a group comprising a central processing unit, a graphics-processing unit, an artificial-intelligence processor, a field-programmable gate array, an application-specific integrated circuit, an application-specific standard product, a system-on-a-chip, a complex programmable logic device, a random-access memory, and a Josephson magnetic random-access memory.

13. The computing system of claim 8, wherein each of the second plurality of components is selected from a group comprising a dynamic random-access memory, a field-programmable gate array, an application-specific integrated circuit, an application-specific standard product, a system-on-a-chip, and a complex programmable logic device.

14. The computing system of claim 8, wherein in each of the plurality of circuits traces comprises a first region including a superconducting metal but excluding a normal metal and a second region including both the superconducting metal and the normal metal.

15. A computing system comprising : a housing, wherein a vacuum is maintained inside the housing; a first plurality of components; a second plurality of components; a first substrate, inside the housing, arranged in a first plane having a first surface and a second surface parallel to the first plane, wherein the second surface is opposite to the first surface, wherein a first set of the first plurality of components is attached to the second surface towards a first end of the first substrate and wherein a second set of the second plurality of components is attached to the second surface towards a second end of the first substrate, wherein the first end is opposite to the second end, wherein each of the first plurality of components is configured to provide primarily a processor functionality and wherein each of the second plurality of components is configured to provide primarily a storage functionality, and wherein a first heat sink is coupled to the first substrate to thermally clamp the first substrate; a second substrate, inside the housing, arranged in a second plane above or below the first plane, the second substrate having a third surface and a fourth surface parallel to the second plane, wherein the fourth surface is opposite to the third surface, wherein a third ser of

the first plurality of components is attached to the fourth surface towards a third end of the second substrate and wherein a fourth set of the second plurality of components is attached to the fourth surface towards a fourth end of the second substrate, wherein the third end is opposite to the fourth end, and wherein each of the first substrate and the second substrate comprising a plurality of circuit traces for interconnecting at least a subset of the first plurality of the components with at least a subset of the second plurality of components, and wherein a second heat sink is coupled to the second substrate to thermally clamp the second substrate and a heat-shield configured to thermally separate the first end from the second end of the first substrate and thermally separate the third end from the fourth end of the second substrate such that each of the first plurality of components is configured to operate at a first temperature and each of the second plurality of components is configured to operate at a second temperature greater than the first temperature and wherein the first temperature is below 9 Kelvin and wherein the second temperature is in a range between 80 Kelvin to 400 Kelvin.

16. The computing system of claim 15, wherein the vacuum corresponds to a pressure in a range between 10^{-3} Torr to 10^{10} Torr.

17. The computing system of claim 15, wherein the primary processor functionality comprises at least one of a central-processing functionality , a graphics-processing functionality, an artificial-intelligence functionality, a gate-array functionality, a memory functionality, or a bus-interface-management functionality.

18. The computing system of claim 15, wherein the primary storage functionality comprises at least one of a memory functionality, gate-array functionality, a bus-management functionality, a controller functionality, or a bus-interface-management functionality.

19. The computing system of claim 15, wherein each of the first plurality of components is selected from a group comprising a central processing unit, a graphics-processing unit, an artificial-intelligence processor, a field-programmable gate array, an application-specific integrated circuit, an application-specific standard product, a system-on-a-chip, a complex programmable logic device, a random-access memory, and a Josephson magnetic random-access memory.

20. The computing system of claim 15, wherein each of the second plurality of components is selected from a group comprising a dynamic random-access memory, a field-programmable gate array, an application-specific integrated circuit, an application-specific standard product, a system-on-a-chip, and a complex programmable logic device.