CLAIMS

1. A method comprising: forming pillars over a substrate; forming conductive material layers and dielectric material layers over the pillars, the conductive material layers being electrically isolated from each other by the dielectric material layers; forming cavities in each of the conductive material layers; and forming a memory element in each of the cavities, wherein forming the cavities includes: forming holes in the conductive material layers and dielectric material layers to form initial cavities in the conductive material layers, wherein the holes are formed such that each of the holes is over a respective pillar among the pillars; and enlarging a size of the initial cavities to form the cavities in each of the conductive material layers.

2. The method of claim 1, wherein each of the conductive material layers is between two of the dielectric material layers and at least one of the conductive material layers is between two of the conductive material layers.

3. The method of claim 1, wherein the memory element comprises polysilicon.

4. The method of claim 1, wherein the memory element comprises a dielectric material.

5. The method of claim 1, wherein second cavities are formed in each of the dielectric material layers when the holes are formed, and a size of the second cavities remains substantially unchanged when the size of the initial cavities the conductive material layers is enlarged.

6. The method of claim 5, wherein each of the second cavities and each of the initial cavities has a substantially same diameter.

7. The method of claim 5, wherein one of the initial cavities is substantially aligned over one of the second cavities.

8. The method of claim 1, wherein the memory element has a ring shape.

9. A method comprising: forming pillars over a substrate; forming conductive material layers and dielectric material layers over the pillars; forming holes in the conductive material layers and dielectric material layers, such that each of the holes is formed over a respective pillar among the pillars; forming cavities in the conductive material layers at locations of the holes, such that each of the cavities has a diameter greater than a diameter of each of the holes; and forming memory cells in the cavities.

10. The method of claim 9, wherein forming the cavities includes: enlarging a size of first cavities formed in the conductive material layers, wherein the first cavities are formed when the holes are formed.

11. The method of claim 9, further comprising: forming conductive channels at locations of the holes, such that each of the conductive channels is in electrical contact with one of the pillars.

12. The method of claim 9, further comprising: forming data lines such that each of the date lines is coupled to multiple pillars among the pillars.

13. The method of claim 12, wherein at least a portion of each of the data lines is formed before the memory cells are formed.

14. The method of claim 9, wherein forming the memory cells includes forming strings of the memory cells, such that memory cells in each of the strings are located in cavities formed from one of the holes.

15. The method of claim 9, wherein forming the memory cells includes forming a dielectric and a memory element in each of the cavities, wherein in a cavity among the cavities, the dielectric is between a sidewall of the cavity and the memory element.

16. The method of claim 9, wherein forming the memory cells includes forming memory elements in the cavities, the memory elements including polysilicon.

17. The method of claim 9, wherein forming the memory cells includes forming memory elements in the cavities, the memory elements including dielectric material.

18. The apparatus of claim 17, wherein the dielectric material including silicon nitride.

19. The method of claim 9, wherein forming the memory cells includes forming memory elements in the cavities, the memory elements including variable resistance material.

20. The method of claim 19, wherein the variable resistance material includes phase change material.