



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H03K 19/094, 19/20	A1	(11) International Publication Number: WO 99/34513 (43) International Publication Date: 8 July 1999 (08.07.99)
(21) International Application Number: PCT/US98/27443 (22) International Filing Date: 22 December 1998 (22.12.98) (30) Priority Data: 08/999,102 29 December 1997 (29.12.97) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): CHAPPELL, Barbara, A. [US/US]; 2710 N.W. Pinnacle Drive, Portland, OR 97225 (US). CHAPPELL, Terry, I. [US/US]; 2710 N.W. Pinnacle Drive, Portland, OR 97225 (US). MILSHTAIN, Mark, S. [US/US]; 221 S.E. 29th, Hillsboro, OR 97123 (US). FLETCHER, Thomas, D. [US/US]; 4785 N.W. 177th Place, Portland, OR 97229 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.
(54) Title: HIGH SPEED RATIOED CMOS LOGIC STRUCTURES FOR A PULSED INPUT		
(57) Abstract		
A logic structure adapted to receive pulsed active input signals produces a logical output with a very small inherent switching delay. In one particular embodiment of the present invention, a logic structure having PFET pullups (402, 406, and 410) and NFET pulldowns (404, 408, and 412), receives active low pulsed input signals (A, B, and C) and produces a logical high output signal (D) when all the input signals are at a low level. When at least one, but not all, of the input signals (A, B, and C) are low, the logic structure produces a logical low output signal (D), while sinking a DC current. When all of the input signals (404, 408, and 412) are at a high level, which is the default condition for this particular embodiment, the logic structure produces a logical low output signal (D), and no DC current paths are switched on.		