

Si/SiGe Vertical Junction Field Effect Transistor

ABSTRACT

A junction field effect transistor and method for making is described incorporating horizontal semiconductor layers within an opening to form a channel (36) and a semiconductor layer through which the opening was made which forms a gate electrode (18,19) surrounding the channel. The horizontal semiconductor layers may be a SiGe alloy with graded composition near the source (21) and drain (15). The invention overcomes the problem of forming low resistance JFET's and provides a gate length that is easily scaleable to submicron dimensions for rf, microwave, millimeter and logic circuits without short channel effect.

Fig. 6