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PARALLEL PLANE SUBSTRATE

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to apparatus and methods for fabricating a conductive substrate. In particular, the present invention relates to a laminated substrate, formed from alternating conductive and dielectric material layers, which may be used as an interposer.

State of the Art: Higher performance, lower cost, increased miniaturization of integrated circuit components, and greater packaging density are ongoing goals of the computer industry. As these goals are achieved, microelectronic dice become smaller. A smaller size allows more microelectronic dice to be produced on each semiconductor wafer, which reduces the cost of each microelectronic die. However, the small size of each microelectronic die makes it difficult to directly incorporate them into microelectronic devices. Thus, a microelectronic die may be attached to an interposer to allow for easier connection of the microelectronic die to other device components.

FIG. 18 illustrates a package 200 comprising a microelectronic die 202 electrically connected to an interposer 204. The interposer 204 comprises a substrate core 206 (e.g., bismaleimide triazine resin, FR4, polyimide materials, and the like) having dielectric layers (e.g., epoxy resin, polyimide, bisbenzocyclobutene, and the like) and conductive traces (e.g., copper, aluminum, and the like) on a top surface thereof to form a top trace network 212, and dielectric layers and conductive traces on a bottom surface thereof to form a bottom trace network 214. To achieve electrical interconnect between the top trace network 212 and the bottom trace network 214, holes are drilled through the substrate core 206 in specific locations and these holes are plated with a conductive material. The resulting plated holes are known in the art as "plated through-hole (PTH)"

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vias 218. FIG. 19 illustrates the interposer 204 with the top trace network 212 and the bottom trace network 214 on the substrate core 206. The top trace network 212 comprises a first dielectric layer 222 having first conductive traces 224 formed thereon, wherein the first conductive traces 224 extend through the first dielectric layer 222 to contact the PTH vias 218 or traces 226 which contact the PTH vias 218. A second dielectric layer 222' is disposed over the first dielectric layer 222 and the first conductive traces 224. Second conductive traces 224' are formed on the second dielectric layer 222', wherein the second conductive traces 224' extend through the second dielectric layer 222' to contact a respective first conductive trace 224. A third dielectric layer 222" is disposed over the second dielectric layer 222' and the second conductive traces 224', and first solder ball lands 228 are formed to extend through the third dielectric layer 222". A first solder resist 232 is formed over the third dielectric layer 222" to surround the first solder ball lands 228. The bottom trace network 214 is formed in a similar fashion as the top trace network 212 with first, second, and third dielectric layers (234, 234', and 234", respectively) and first, second, and third conductive traces (236, 236', and 236", respectively), wherein second solder ball lands 238 are formed with the third conductive traces 236" and a second solder resist 242 is formed over the third dielectric layer 234" and a portion of the third conductive trace 236" to surround the second solder ball lands 238.

Referring to FIG. 18, the microelectronic die 202 is attached to and in electrical contact with the top trace network 212 through small solder balls 244. The small solder balls 244 extend between contacts 246 on the microelectronic die 202 and the first solder ball lands 228 (see FIG. 19). External contacts 248 (shown as solder balls) are formed on the second solder ball lands 238 (see FIG. 19). The external contacts 248 are attached to an external electrical system (not shown). Thus, the use of the interposer 204

allows electrical communication between the microelectronic die 202 and an external electrical system (not shown).

FIGs. 20-24 illustrate a panel plating method of forming a copper plated through-hole via, such as shown as the PTH vias 218 in FIGs. 18 and 19. As shown in FIG. 20, a first copper layer 252 disposed on a first surface 254 of the substrate 206 and a second copper layer 256 disposed on a second surface 258 of substrate 206. A hole 262 is drilled through the first copper layer 252, the substrate 206, and the second copper layer 256, as shown in FIG. 21. As shown in FIG. 22, a copper sidewall layer 264 is formed on a sidewall(s) 266 of the hole 262 with an electroless copper plating technique followed by a copper electroplating process, as known in the art. A resist layer 268 is patterned over the hole 262 (see FIG. 22) and a portion of the first copper layer 252 and the second copper layer 256, as shown in FIG. 23. The first copper layer 252 and the second copper layer 256 are then etched and the resist layer 268 is removed to form a plated through-hole via 218, as illustrated in FIG. 24.

The fabrication of the interposer 204 requires a number of processing steps which increases the cost of the package. In particular, the formation of the PTH vias 218 has numerous, time-intensive processing steps. Therefore, it would be advantageous to design an interposer and a technique for fabrication the same, which eliminates the need for forming PTH vias.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is an oblique view of a parallel conducting plane substrate block, according to the present invention;

FIG. 2 is a side cross-sectional view of the parallel plane substrate block of FIG. 1, according to the present invention;

FIG. 3 is an oblique view of a parallel plane substrate having been cut from the block of FIG. 1, according to the present invention;

FIG. 4 is a side cross-sectional view of a parallel plane substrate, according to the present invention;

FIGs. 5-12 are side cross-sectional views of a method of forming an interposer using a parallel plane substrate, according to the present invention;

FIG. 13 is a side cross-sectional view of a microelectronic package, according to the present invention;

FIG. 14 is an oblique view of a first alternate substrate layer, according to the present invention;

FIG. 15 is an oblique view of a second alternate substrate layer, according to the present invention;

FIG. 16 is an oblique view of an alternate parallel plane substrate having been cut from a block including the first alternate substrate layers of FIG. 14 and the second alternate substrate layers of FIG. 15, according to the present invention;

FIG. 17 is a side cross-sectional view of a microelectronic package, according to the present invention;

FIG. 18 is a side cross-sectional view of a microelectronic package, as known in the art;

FIG. 19 is a side cross-sectional view of a plated through-hole via in the interposer and the top and bottom trace networks of FIG. 18, as known in the art; and

FIGs. 20-24 are side cross-sectional views of a method of fabricating a plated through-hole via, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable though skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implement within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views. Furthermore, the drawings are not meant illustrate any scale of the present invention but are merely illustrative of the general concept of the present invention.

FIG. 1 illustrates a parallel plane substrate block 100, according to the present invention. The parallel plane substrate block 100 comprises alternating substrate dielectric material layers 102 and substrate conductive material layers 104. The substrate dielectric material layers 102 may include, but are not limited to, filled epoxy

resin, FR4, polyimide, bisbenzocyclobutene, ceramic materials, and the like. The substrate conductive material layers 104 may include, but are not limited to, copper, copper alloys, aluminum, aluminum alloy, tungsten, tungsten alloys, and the like. The parallel plane substrate block 100 may preferably be between about 2" and 12" thick 106, high 107, and deep 108.

As shown in FIG. 2, the substrate block 100 is formed by providing a first layer of substrate dielectric material 102_1 and disposing a first substrate conductive material layer 104_1 over said first substrate dielectric material 102_1. A second substrate dielectric material layer 102_2 is disposed over the first substrate conductive material layer 104_1 and a second substrate conductive material layer 104_2 is disposed over the second substrate dielectric material layer 102_2. This process is repeated until a desired number of substrate dielectric material layers 102_n and a desired number of substrate conductive material layers 104_{n-1} are formed. This results in the formation of the substrate block 100 that is essentially a lamination of dielectric and conductive material layers. It is, of course, understood that each substrate dielectric material layer 102 may comprise a plurality of dielectric material layers, and that each substrate conductive material layer 104 may comprise a plurality of conductive material layers.

Preferably, a filled epoxy resin is deposited with a thin copper foil disposed thereon in a sequential lamination repeated to form a 25-layer block (12 layers of copper foil and 13 layers of filled epoxy resin). Thereafter, the 25-layer blocks are pressed in a lamination process well known to those experienced in the art. Individual 25-layer blocks are then aligned with one another and laminated to each other to form the parallel plane substrate block 100. Other means of lamination with block layer counts of greater than or less than 25 are possible. The critical factor required during lamination is the

maintenance of a well-controlled dielectric material thickness, which is uniform between the many layers contained in the block.

As shown in FIG. 3, the substrate block 100 is sliced perpendicular to the laminated substrate dielectric material layers 102 and substrate conductive material layers 104 to form a parallel plane substrate 110. Slicing the parallel plane substrate 110 in this manner results in each of the substrate dielectric material layers 102 and each of the substrate conductive material layers 104 extending from a first surface 116 of the parallel plane substrate 110 to an opposing second surface 130 of the parallel plane substrate 110 (shown in FIG. 5). The slicing may be achieved with any appropriate cutting device known in the art, including but not limited to, diamond saws and water saws. The parallel plane substrate 110 preferably has a thickness 112 of between about 0.5 mm and 3 mm, most preferably about 1 mm. As shown in FIG. 4, the parallel plane substrate 110 is preferably designed such that the substrate conductive material layers 104 are on approximately a 0.3175 mm (12.5 mil) pitch "A" in order to assist in forming a 50 mil pitch ball grid array package, as known in the art. Preferably, the substrate dielectric material layers 102 have a thickness "B" of about 0.2825 mm (11.12 mils) and the substrate conductive material layers 104 have a thickness "C" of about 0.035 mm (1.38 mils).

The parallel plane substrate 110 may be used as a substrate core in an interposer. FIGs. 5-12 illustrate the fabrication of such an interposer. As shown in FIG. 5, at least one conductive land 111 is formed on the parallel plane substrate first surface 116 at desired locations. The conductive lands 111 contact individual respective substrate conductive material layers 104 in a substantially perpendicular orientation. The conductive lands 111 may be formed by any technique known in the art. Preferably, the conductive lands 111 are formed of copper with any known panel plating technique.

As shown in FIG. 6, a first dielectric material layer 114 is the disposed over the parallel plane substrate first surface 116 and the conductive lands 111. As shown in FIG. 7, at least one via 118 is formed through the first dielectric material layer 114 to expose at least a portion of at least one substrate conductive material layer 104. The vias 118 can be formed by any known technique including, but not limited to, laser drilling and etching.

A first resist layer 122 is then patterned on the first dielectric material layer 114, as shown in FIG. 8. At least one first conductive trace 124 is formed on portions of the first dielectric material layer 114 not covered by the patterned first resist layer 122 and extends through the first dielectric material layer 114 to contact a respective substrate conductive material layer 104, as shown in FIG. 9. As shown in FIG. 10, a second dielectric material layer 114' is disposed over the first dielectric material layer 114 and the first conductive traces 124. As shown in FIG. 11, at least one second conductive trace 124' is formed on the second dielectric material layer 114' using a patterned second resist layer 122', in a manner previously described. The second conductive traces 124' extend through the second dielectric material layer 114' to contact a respective first conductive trace 124. A third dielectric material layer 114" is disposed over the second resist layer 122' and the second conductive traces 124'. First solder ball lands 126 (illustrated as a trace 127 having solder 129 disposed thereon) are formed using a patterned third resist layer 122" to extend through the third dielectric material layer 114". A first solder resist 128 may be formed over the third resist layer 122" to surround the first solder ball lands 126, thus forming a top trace network 144. It is, of course, understood the each of the first resist layer 122, the second resist layer 122', and the third resist layer 122" could have been removed.

As shown in FIG. 12, a bottom trace network 146 may be formed on the parallel plane substrate second surface 130 in a similar fashion as the top trace network 144 with conductive lands 131, first, second, and third dielectric material layers (132, 132', and 132", respectively), first, second, and third resist layers (134, 134', and 134", respectively), and first, second, and third conductive traces (136, 136', and 136", respectively), wherein second solder ball lands 142 are formed with the third conductive traces 136" and a second solder resist 138 is formed over the third resist layer 134" and a portion of the third conductive trace 136" to surround the second solder ball lands 142. This results in an interposer 148, as shown in FIG. 12. It is, of course, understood that although three layers of dielectric material and conductive traces are illustrated, the present invention is not so limited. There may be any number of such layers greater or less than three.

It is noted that the first conductive trace 124 of the top trace network 144 need not be vertically aligned with a corresponding first conductive trace 136 of the bottom trace network 146 (between which electrical communication is desire). The first conductive trace 114 of the top trace network 144 and its corresponding first conductive trace 136 of the bottom trace network 146 need only contact a common substrate conductive material layer 104 anywhere along a length (perpendicular to FIG. 12) of the substrate conductive material layer 104.

FIG. 13 illustrates a microelectronic package 150 comprising a microelectronic die 152 is attached to and in electrical contact with the top trace network 144 of the parallel plane substrate 110 through small solder balls 154. The small solder balls 154 extend between contacts 156 on the microelectronic die 152 and the first solder ball lands 126 (see FIG. 12) of the top trace network 144. External contacts 158 (shown as solder balls) are formed on the second solder ball lands 142 (see FIG. 12) of the bottom trace

network 146. Of course, this invention is not limited to microelectronic dice 152 connected through solder balls 154, as illustrated in FIG 13. The microelectronic die 152 can be connected through wire bonds or other connection technique known to those familiar with the art.

It is, of course, understood that multiple microelectronic dice could be connected to discrete top trace networks on a large parallel plane substrate 110, which is diced to form discrete packages, such as shown in FIG. 13.

The present invention is not limited to the substrate conductive material layer 104 being a conductive across the entire layer. For example, one embodiment of the present invention may be a first intermittent conductive material layer 160, as illustrated in FIG. 14. The first intermittent conductive material layer 160 comprises a dielectric substrate 165 (such as a FR4 or BT resin substrate) having alternating sections of conductive material 162 (such as copper), for example about 0.1651 mm (6.5 mils) wide 166, and dielectric material 164 (such as filled epoxy resin), for example about 0.1524 mm (6.0 mils) wide 168, formed thereon. The first intermittent conductive material layer 160 itself may be about 0.3175 mm thick 170. The first intermittent conductive material layer 160 may be fabricated in the same manner as a single layer printed circuit boards are fabricated using standard print circuit board fabrication equipment, as well known in the art. As will be seen, the use of intermittent conductive material layer 160 in the fabrication of a substrate results discrete conductive vias extending through the substrate rather than a conducting plane as with the embodiment shown in FIG. 3.

Furthermore, the conductive material width 166 or the dielectric material width 168 may be varied. As illustrated in FIG. 15, a wide section of conductive material 172, for example about 16.9 mm (665.4 mils) wide 174 may be fabricated amid the alternating sections the conductive material 162 and the dielectric material 164 as

described in FIG. 14 to form a second intermittent conductive material layer 176. The wide section of conductive material 172 may be used to carry a power supply (preferably located directly below a microelectronic die in a final assembly) and the sections of conductive material 162 may be used to carry electronic signals.

FIG. 16 illustrates an oblique view of a substrate 178 having been cut from substrate block 180 which has incorporated the first intermittent conductive material layer 160 and the second intermittent conductive material layer 176 embodiments, as illustrated in FIGs. 14 and 15, and may include planar conductive material layers 182 (similar to substrate conductive material layer 104 of FIGs. 1-13). The first intermittent conductive material layers 160, the second intermittent conductive material layers 176, and the planar conductive material layers 182 are separated by dielectric material layers 184.

As shown in FIG. 17, a microelectronic package 190 may be fabricated by forming a top trace network 186 and a bottom trace network 188 on a substrate 195 similar to that shown in FIG. 16 to fabricate an interposer 192 (similar to interpose 148, as shown in FIG. 12). A microelectronic die 194 is attached to and in electrical contact with the top trace network 186 through small solder balls 196. The small solder balls 196 extend between contacts 197 on the microelectronic die 194 and the top trace network 186. External contacts 198 (shown as solder balls) are formed on the bottom trace network 188.

With regard to the present invention in general, due to the placement of numerous parallel planes in close proximity to each other, the current supplied to the microelectronic die for the purpose of supplying power, follows a path of lower inductance and lower resistance than would be typical in a standard multilayer package with plated through holes. In addition, the signal traces going through the parallel plane

core are shielded from one another in a manner that is superior to that in a standard multilayer package with plated through holes. As illustrated in FIG. 16, this results from the fact that the signal traces going through the parallel plane core are surrounded on all four sides by a reference plane held at either the ground or supply voltage level. This isololation is not possible in a standard multilayer package with plated through holes.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic substrate, comprising:

a plurality of alternating substantially planar layers of substrate dielectric material and substrate conductive material; and

a first surface and a second surface wherein said plurality of alternating substantially planar layers of substrate dielectric material and substrate conductive material extend substantially perpendicularly between said first surface and said second surface.

2. The microelectronic substrate of claim 1, wherein said substrate dielectric material layers is selected from the group consisting of filled epoxy resin, FR4 material, polyimide, and bisbenzocyclobutene.

3. The microelectronic substrate of claim 1, wherein said substrate conductive material layers is a conductive material selected from the group consisting of copper, aluminum, and alloys thereof.

4. The microelectronic substrate of claim 1, wherein said substrate conductive material layers comprises at least one continuous conductive material layer.

5. The microelectronic substrate of claim 1, wherein said substrate conductive material layer comprises at least one intermittent conductive material layer.

6. The microelectronic substrate of claim 5, wherein said at least one intermittent conductive material layer comprises alternating sections of conductive material and dielectric material.

7. A microelectronic device, comprising:

a substrate having a first surface and a second surface;

said substrate comprising a plurality of alternating substantially planar layers of substrate dielectric material and substrate conductive material, wherein each substrate dielectric material layer and each substrate conductive material layer extend substantially perpendicularly between said substrate first surface and said substrate second surface; and

a trace network disposed on at least one of said substrate first surface and said substrate second surface.

8. The microelectronic device of claim 7, wherein said trace network comprises at least one dielectric layer disposed on said substrate first surface, and further including at least one conductive trace disposed on and extending through said at least one first surface dielectric layer to contact at least one substrate conductive material layer.

9. The microelectronic device of claim 8, further including a trace network disposed on said substrate second surface comprising at least one conductive trace disposed on said at least one second surface dielectric layer and extending through said

at least one second surface dielectric layer to contact at least one substrate conductive material layer.

10. The microelectronic device of claim 7, wherein said substrate dielectric material layers is selected from the group consisting of filled epoxy resin, FR4 material, polyimide, and bisbenzocyclobutene.

11. The microelectronic device of claim 7, wherein said substrate conductive material layers is a conductive material selected from the group consisting of copper, aluminum, and alloys thereof.

12. The microelectronic device of claim 7, wherein said substrate conductive material layers comprises at least one continuous conductive material layer.

13. The microelectronic device of claim 7, wherein said substrate conductive material layer comprises at least one intermittent conductive material layer.

14. The microelectronic device of claim 13, wherein said at least one intermittent conductive material layer comprises alternating sections of conductive material and dielectric material.

15. A method of fabricating a microelectronic substrate, comprising:

layering alternating substantially planar dielectric material layers and conductive material layers to form a block;

slicing a section from said block perpendicular to said planar dielectric material layers and said conductive material layers.

16. The method of claim 15, wherein layering said conductive layers comprises layering at least one continuous conductive material layer.

17. The method of claim 15, wherein layering said conductive layers comprises layering at least one intermittent conductive material layer.

18. The microelectronic substrate of claim 17, wherein layering said at least one intermittent conductive material layer comprises layering said at least one intermittent conductive material layer having alternating sections of conductive material and dielectric material.

19. A method of fabricating a microelectronic device, comprising:

layering alternating substantially planar dielectric material layers and conductive material layers to form a block;

slicing a section from said block perpendicular to said planar dielectric material layers and said conductive material layers to provide a substrate having a first surface and a second surface; and

disposing a trace network on at least one of said substrate first surface and said substrate second surface.

20. The method of claim 19, wherein disposing said trace network comprises disposing at least one dielectric layer on said substrate first surface, and further including

disposing at least one conductive trace on and extending through said at least one first surface dielectric layer to contact at least one substrate conductive material layer.

21. The method of claim 20, further including disposing a second trace network on said substrate second surface comprising at least one conductive trace disposed on said at least one second surface dielectric layer and extending through said at least one second surface dielectric layer to contact at least one substrate conductive material layer.

22. The method of claim 19, further including atttaching at least one microelectronic die attached to said trace network.

23. The method of claim 19, wherein layering said conductive layers comprises layering at least one continuous conductive material layer.

24. The method of claim 19, wherein layering said conductive layers comprises layering at least one intermittent conductive material layer.

25. The method of claim 19, wherein layering said at least one intermittent conductive material layer comprises layering said at least one intermittent conductive material layer having alternating sections of conductive material and dielectric material.