

CLAIMS

What is claimed is:

- 1 1. A method of fabricating an electronic device comprising:
2 forming, on a substrate, a first electrode layer and a first self-selecting memory
3 stack on the first electrode layer;
4 etching, in a first etching operation, the first electrode layer and the first self-
5 selecting memory stack to form a first set of rows extending in a first direction on the
6 substrate, each row of the first set of rows comprising remaining portions of the first
7 electrode layer and the first self-selecting memory stack;
8 forming a second electrode layer and a second self-selecting memory stack on
9 the first set of rows;
10 etching, in a second etching operation, the second electrode layer and the
11 second self-selecting memory stack to form a first set of columns extending in a second
12 direction on the first set of rows, each column of the first set of columns comprising
13 remaining portions of the second electrode layer and the second self-selecting memory stack;
14 and
15 etching, in the second etching operation, portions of the first set of rows
16 located between adjacent columns of the first set of columns to form a first set of memory
17 cells.
- 1 2. The method of claim 1, further comprising:
2 forming a third electrode layer on the first set of columns;
3 etching, in a third etching operation, the third electrode layer to form a second
4 set of rows extending in the first direction on the first set of columns, each row of the second
5 set of rows comprising the third electrode layer; and
6 etching, in the third etching operation, portions of the first set of columns
7 located between adjacent rows of the second set of rows to form a second set of memory
8 cells.
- 1 3. The method of claim 1, further comprising:
2 forming a third electrode layer and a third self-selecting memory stack on the
3 first set of columns;
4 etching, in a third etching operation, the third electrode layer and the third
5 self-selecting memory stack to form a second set of rows extending in the first direction on

6 the first set of columns, each row of the second set of rows comprising the third electrode
7 layer and the third self-selecting memory stack; and
8 etching, in the third etching operation, portions of the second set of rows
9 located between adjacent columns of the first set of columns to form a second set of memory
10 cells.

1 4. The method of claim 3, further comprising:
2 forming a fourth electrode layer on the second set of rows;
3 etching, in a fourth etching operation, the fourth electrode layer to form a
4 second set of columns extending in the second direction on the second set of rows, each
5 column of the second set of columns comprising the fourth electrode layer; and
6 etching, in the fourth etching operation, portions of the second set of rows
7 located between adjacent columns of the second set of columns to form a third set of memory
8 cells.

1 5. The method of claim 1, wherein each self-selecting memory stack
2 comprises a first layer of barrier material below and in contact with a layer of chalcogenide
3 glass and a second layer of barrier material above and in contact with the layer of
4 chalcogenide glass.

1 6. The method of claim 5, wherein the second etching operation
2 comprises:
3 etching through the second self-selecting memory stack and through a portion
4 of the first self-selecting memory stack below and between adjacent columns of the first set
5 of columns;
6 detecting the first layer of barrier material in contact with a first layer of
7 chalcogenide glass has been reached in the second etching operation, the first self-selecting
8 memory stack comprising the first layer of chalcogenide glass; and
9 stopping the second etching operation.

1 7. The method of claim 5, wherein the second etching operation
2 comprises:
3 etching through the second self-selecting memory stack and through a portion
4 of the first self-selecting memory stack below and between adjacent columns of the first set
5 of columns;

6 detecting the second layer of barrier material in contact with a first layer of
7 chalcogenide glass has been reached in the second etching operation, the first self-selecting
8 memory stack comprising the first layer of chalcogenide glass; and
9 stopping the second etching operation.

1 8. The method of claim 1, wherein a width of each column of the first set
2 of columns is a same width as a width of each respective memory element located under each
3 column of the first set of columns.

1 9. The method of claim 8, wherein the width of each column is a same
2 width as the width of each row.

1 10. The method of claim 8, wherein the width of each column is a different
2 width as the width of each row.

1 11. The method of claim 1, wherein the second electrode layer forms an
2 upper access line for a column of memory cells of the first set of memory cells that are
3 located under each column of the first set of columns, and forms a lower access line for a
4 second column of a second set of memory cells formed using the second self-selecting
5 memory stack.

1 12. The method of claim 11, wherein second electrode is formed in a
2 single deposition process and is etched in a single etching process as part of the second
3 etching operation.

1 13. The method of claim 1, wherein the first self-selecting memory stack
2 comprises a first layer of chalcogenide glass for both selection and storage and the second
3 self-selecting memory stack comprises a second layer of chalcogenide glass for both selection
4 and storage.

1 14. The method of claim 13, wherein the first etching operation exposes a
2 sidewall of the first self-selecting memory stack and the second etching operation exposes a
3 sidewall of the second self-selecting memory stack, the method further comprising:
4 forming a first sealing layer in contact with the sidewall of the first self-
5 selecting memory stack, the first sealing layer configured to maintain a chemical composition
6 of the first layer of chalcogenide glass; and

7 forming a second sealing layer in contact with the sidewall of the second self-
8 selecting memory stack, the second sealing layer configured to maintain a chemical
9 composition of the second layer of chalcogenide glass.

1 15. The method of claim 14, further comprising:
2 depositing, after forming the first sealing layer, a dielectric material between
3 rows of the first set of rows; and
4 depositing, after forming the second sealing layer, the dielectric material
5 between columns of the first set of columns.

1 16. The method of claim 15, further comprising:
2 forming the first sealing layer and the second sealing layer at a first
3 temperature; and
4 depositing the dielectric material at a second temperature that is greater than
5 the first temperature.

1 17. A memory device, comprising:
2 a first array of memory cells that each comprise a first self-selecting memory
3 element, the first array of memory cells having a first plurality of columns extending in a first
4 direction and a first plurality of rows extending in a second direction; and
5 a second array of memory cells that each comprise a second self-selecting
6 memory element, the second array of memory cells having a second plurality of columns
7 extending in the first direction and a second plurality of rows extending in the second
8 direction, wherein the second array overlies the first array, each of the second plurality of
9 columns overlay respective columns of the first plurality of columns, and a width of each
10 column of the first plurality of columns is a same width as a width of each respective column
11 of the second plurality of columns.

1 18. The memory device of claim 17, further comprising:
2 a first plurality of access lines coupled with a lower portion of each memory
3 cell of each row of the first plurality of rows;
4 a second plurality of access lines coupled with an upper portion of each
5 memory cell of each column of the first plurality of columns and coupled with a lower
6 portion of each memory cell of each column of the second plurality of columns; and

7 a third plurality of access lines coupled with an upper portion of each memory
8 cell of each row of the second plurality of rows.

1 19. The memory device of claim 18, wherein the first plurality of columns,
2 the second plurality of access lines, and the second plurality of columns are self-aligned.

1 20. The memory device of claim 18, wherein the first plurality of columns,
2 the second plurality of access lines, and the second plurality of columns have a same
3 patterning registration and a same width.

1 21. The memory device of claim 18, wherein the second plurality of access
2 lines comprise a metal material with an absence of an intra-layer boundary.

1 22. The memory device of claim 17, wherein the first self-selecting
2 memory element comprises a first layer of chalcogenide glass for both selection and storage
3 and the second self-selecting memory element comprises a second layer of chalcogenide
4 glass for both selection and storage.

1 23. The memory device of claim 22, further comprising:
2 a first sealing layer in contact with a sidewall of the first self-selecting
3 memory element, the first sealing layer configured to maintain a chemical composition of the
4 first layer of chalcogenide glass; and
5 a second sealing layer in contact with a sidewall of the second self-selecting
6 memory element, the second sealing layer configured to maintain a chemical composition of
7 the first layer of chalcogenide glass.

1 24. The memory device of claim 23, further comprising:
2 a dielectric material deposited adjacent to the first sealing layers; and
3 the dielectric material deposited adjacent to the second sealing layers.

1 25. A memory device, comprising:
2 a plurality of pillars arranged in a three-dimensional cross-point architecture
3 with a first access line, a second access line, and a third access line, each pillar comprising:
4 a first memory storage element coupled to the first access line and the
5 second access line; and

6 a second memory storage element coupled to the second access line
7 and the third access line,
8 wherein the first memory storage element, the second access line, and
9 the second memory storage element are self-aligned in a first direction corresponding
10 to a width of the respective pillar.

1 26. The memory device of claim 25, wherein the second memory storage
2 element has a second width in a second direction substantially orthogonal to the first
3 direction, the second width different from the width of the respective pillar in the first
4 direction.

1 27. The memory device of claim 25, wherein each of the first memory
2 storage element and the second memory storage element comprise a self-selecting memory
3 storage element.

1 28. The memory device of claim 25, wherein the first memory storage
2 element and the second memory storage element each comprise a chalcogenide glass.

1 29. The memory device of claim 25, wherein the first memory storage
2 element comprises a first deck of a three-dimensional cross point memory architecture and
3 the second memory storage element comprises a second deck of the three-dimensional cross
4 point memory architecture.

1 30. The memory device of claim 25, wherein the second access line
2 comprises a metal material with an absence of an intra-layer boundary.

1 31. A method of fabricating an electronic device comprising:
2 forming, on a substrate, control circuitry for controlling a plurality of stacked
3 decks of a three-dimensional cross point memory, the plurality of stacked decks comprising
4 N decks; and
5 forming, over at least a portion of the control circuitry, at least a portion of the
6 plurality of stacked decks using N+1 mask operations and N+1 etch operations.

1 32. The method of claim 31, wherein forming the plurality of stacked
2 decks comprises:

3 forming a first plurality of rows of a first deck of the stacked decks of the
4 plurality that each comprise a first electrode layer and a first self-selecting memory stack;
5 forming a second electrode layer on the first plurality of rows and a second
6 self-selecting memory stack on the second electrode layer;
7 patterning a first plurality of columns on the second self-selecting memory
8 stack; and
9 etching, in a single etching operation, the second self-selecting memory stack,
10 the second electrode layer, and portions of the first self-selecting memory stack that are
11 located between adjacent columns of the first plurality of columns.

1 33. An electronic memory apparatus, comprising:
2 a first memory cell that includes a first self-selecting memory storage element
3 coupled between a first access line and a second access line;
4 a second memory cell that includes a second self-selecting memory storage
5 element, the second memory cell coupled between the second access line and a third access
6 line; and
7 a controller in electronic communication with the first memory cell and the
8 second memory cell, wherein:
9 the second self-selecting memory storage element overlies the first
10 self-selecting memory storage element, and
11 the second access line comprises a metal material with an absence of
12 an intra-layer boundary.

1 34. The electronic memory apparatus of claim 33, wherein the first self-
2 selecting memory storage element, the second self-selecting memory storage element and the
3 second access line have a same width in a first direction.

1 35. The electronic memory apparatus of claim 33, wherein the second self-
2 selecting memory storage element has a second width in a second direction, substantially
3 orthogonal to a first direction, that is different than a first width in the first direction.

1 36. The electronic memory apparatus of claim 33, wherein the first self-
2 selecting memory storage element, the second self-selecting memory storage element and the
3 second access line are self-aligned in a first direction.