"Forming an electrical contact on an electronic component."

This invention relates to a method of forming an electrical contact on an electronic component, such as the semiconductor chip or substrate of an electronic component package, particularly for application in flip-chip technology.

With the increasing density of devices on a semiconductor chip and ever more complex applications there is a need to form ever smaller and more precise electrical connections when packaging such semiconductor chips, especially medium and higher end products with high input/output counts.

In one conventional method, electrical connections in packaged electronic components are made using electrical contacts in the form of solder bumps which are deposited by a solder deposition process on contact pads of one of two components to be interconnected, the solder deposition process requiring special alignment techniques, such as the application of a masking resist to the surface of the component to define the individual locations at which solder bumps are to be deposited. The masking layer then has to be subsequently removed after the solder has been deposited on the surface.

In another known method, solder paste is screen printed on the contact pads of a component using a metal mask. The use of such metal masks means that accurate alignment techniques are required to deposit the paste on individual pads and the chance of bridging between pads increases as the pitch decreases.

In yet another known process for making electrical connections, a contact on one component is connected to a metal stud on another components using an electrically conducting adhesive material which contains metal particles. Because only a few of the metal particles in the adhesive material make an electrical connection with the stud, the electrical resistance of such an connection is rather high.

With the ever smaller size, higher packing density and complexity of semiconductor devices in semiconductor chips, the electronic component packaging industry is increasingly being faced with the need to provide more closely packed electrical connections of smaller and smaller area whilst maintaining the electrical isolation and integrity of the individual connections.

Because the required dimensions of solder joints are therefore steadily shrinking and solders have an intrinsically low melting point, the electrical resistance, the mechanical strength and the susceptibility of such joints to electro-migration are becoming increasingly important factors.

It is becoming increasingly troublesome to form satisfactory connections of the required small size and at the required small pitch using these known connection-forming techniques. For example, it is extremely difficult and relatively expensive to form solder bumps by conventional methods with a bump size of 75 μm or less at a pitch of 125 μm or less.

It is an object of the present invention to provide a method of forming an electrical contact on an electronic component which enables strong, low resistance connections of high integrity to be reliably constructed with a size of 100 μm or less and a pitch of 150 μm or less.

Accordingly, in one aspect, the invention provides a method of constructing a an electrical contact on an electronic component, comprising providing a protruding electrically conducting core on the component at a site where an electrical connection is to be made, and dipping the core in molten solder, without using a mask, so that the solder adheres to the core and forms a solder bump on the core.

In another aspect, the invention provides a method of electrically interconnecting two electronic components, comprising forming an electrical contact on a contact pad of one of the components using the method of the invention and forming a bond between the electrical contact thus formed and a contact pad of the other component.

In a further aspect, the invention provides an electronic component having an electrical contact formed in accordance with the method of the invention and having a protruding electrically conducting core and a solder bump formed on and adhering to the core.

In yet another aspect, the invention provides an electronic components package comprising a semiconductor chip and a mounting substrate, in which one of the chip and the substrate is a component having electrical contacts formed in accordance with the method of the invention, and the other of the chip and substrate has contact pads bonded to the electrical contacts of the one component by the solder bumps of the contacts.

In order that the invention may be more readily understood, an embodiment thereof will now be described, by way of example, with reference to the accompanying illustrations, in which:

Figure 1 is a plan view of an electronic component embodying the present invention in the form of a semiconductor test chip having electrical contacts formed by a method embodying the invention;

Figure 2 is a plan view of the surface of the electronic component on an enlarged scale, showing the fine pitch which can be achieved by the method embodying the invention between adjacent electrical contacts in a row of such contacts;

Figure 3 is on a still larger scale and shows the integrity and good electrical isolation which can be achieved between adjacent electrical contacts formed in accordance with the method embodying the invention;

Figure 4 is a view from above of a row of electrical contacts formed by the method embodying the present invention;

Figures 5 is a schematic representation of a solder bond formed between a substrate and a semiconductor chip using an electrical contact provided on the chip by the method embodying the present invention;

Figure 6 is a cross-section taken through an electrical contact formed by the method embodying the invention; and

Figures 7 and 8 illustrate the results of shear testing an electrical contact of an electronic component provided with such contact by the method embodying the invention.

In one embodiment of the method of the present invention, protruding electrically conducting cores in the form of solid metal studs 1 (see Figures 4, 5 and 6) are fabricated on contact pads 2 of a semiconductor chip 3 which is to be electrically interconnected with a mounting substrate, which may be an organic substrate, in the manufacture of a packaged electronics product. The contact pads 2 are commonly made of aluminium or copper and may possibly be coated with other materials. The studs 1 are formed from gold wire of 25.4 μm diameter secured to the contact pads by means of a conventional wire bonding technique. The studs may be coined after they have been formed on the chip or may be left plain. Although the stud configurations shown in the drawings are linear arrays, both linear and two-dimensional stud arrays may be fabricated.

The projecting gold studs 1 thus formed on the contact pads 2 are then brought into contact with molten solder, for example by dipping in a solder bath, whereupon it is found that the solder selectively wets and adheres only to the studs and not to the other areas of the semiconductor chip 3. This selective wetting of the metal studs by the solder effectively self-alignes the solder deposits without the need for any additional alignment steps, such as the application and development of photo-resists or application of some other kind of mask, e.g. a metal mask.

Figures 1 to 5 show the electrical contacts 5 which are formed after dipping in molten solder and which comprise solder bumps 4 deposited on and adhering to the gold studs 1 fabricated on the aluminium pads 2 of the semiconductor test chip 3. As will be seen from the Figures, the solder only wets and adheres to the gold studs 1, leaving the aluminium pads 2 and the passivation surface 6 of the semiconductor chip 3 free of solder.

Figures 2 and 3 show that electrical contacts 5 formed in accordance with a method embodying the invention may be fabricated in close proximity to one another whilst still maintaining their structural and electrical integrity. In particular, Figures 2 and 3 show that contacts 5 having solder bumps 4 with a dimension of 75 μm can be fabricated without any solder bridging between the solder bumps, this bump dimension being comparable to or better than those achievable by the known processes currently used by the electronic component packaging industry.

Figure 4 shows that solder can be selectively deposited with good accuracy on the top part of the gold stud 1.

After forming contacts 5 on a test chip 3 as described above, the chip was assembled with a substrate 7 (see Figure 5). To this end, input/output pads 8 provided on the substrate 7 are masked with a solder mask 9 and joined to the solder bumps 4 of the electrical contacts 5 of the chip 3 to form solder joints which electrically interconnect the pads 2 and 8 of the chip 3 and substrate 7 as desired. In the resulting assembly, the solder bumps 4 of the chip contacts 5 formed a robust metallic bond with the input/output pads 8 of the substrate 7.

To test the reliability of the interconnections, the electrical contacts 5 were subjected to a microscopy study and shear tests were conducted on the electrical contacts using an ASTM (American Society for Testing Materials) standard method.

Figure 5 shows a schematic cross-section through the electrical contacts 5 formed on the chip 3 by the studs 1 with the solder bumps 4 adhering thereto. The shear tests revealed that the contacts had shear strengths well above the minimum acceptable value. Moreover, as illustrated in Figures 6 and 7, the

shear tests applied to the contacts 5 resulted in fractures 6 occurring at the interface between the chip pads 2 and the silicon of the semiconductor chip 3, suggesting the existence of a very robust interface between the electrical contacts 5 and the pads 2 as well as strength within the contacts 5 themselves.

Whilst in the above described embodiment the electrical contacts are formed on a semiconductor chip they could, of course equally be formed on the substrate or on some other electronic component with which a solder joint is to be formed.

Although the studs in the described embodiment are made of gold, this is but one example of an electrically conducting material which can be used to form the solid core of a solder contact embodying the invention. In particular, wires of copper, silver, platinum, palladium or nickel or their alloys may be used to construct the electrically conducting studs on which the solder bumps are deposited to form the electrical contacts. Furthermore, it is envisaged that wires made of any other suitable material coated with gold, copper, silver, platinum, palladium or nickel or their alloys could be used to construct the electrically conducting studs. Moreover, it is envisaged that a plurality of studs may be stacked by wire bonding to increase the height of the resulting solder joint.

The formation of the solder bumps on the electrically conducting studs may be performed using any suitable process, such as dipping in a solder bath as described above or, for example, by wave soldering. If desired or necessary in any particular case, the studs may also be contacted with the solder a plurality of times in order to build the solder bump up to a required size.

It will be appreciated that electrical contacts embodying the present invention can be fabricated at relatively low cost using only equipment which is already

standard in the electronic component packaging industry. In addition, the solder bumps are deposited on the studs by a self-aligning process which obviates the need to use masks to define the locations of the solder deposits, so that the method of fabricating the contacts is in fact simpler in this respect than existing methods.

The use of contacts embodying the invention enables the formation of high strength bonds during assembly, even with electrical contacts having a dimension of 75 μm or less, due to the combined effects of the mechanical support provided by the solid stud itself and a measure of solute alloying of the stud material which occurs when the molten solder is deposited on the stud. The solute alloying of the stud material into the solder of the solder bump also enhances the resistance of the contact to electromigration, a potentially serious problem as the size of solder joints decreases.

The high strength and the integrity of contacts embodying the invention significantly reduce the chances of the contacts collapsing during assembly, one of the main factors in reducing yields in the electronic component packaging industry. Moreover, the method by which such contacts are formed means that solder bumps having dimensions of 75 μm or less can be reliably produced at a pitch of 150 μm or less, thereby allowing the input/output counts of packaged semiconductor chips to be increased.

It is envisaged that, where the component on which the electrical contacts are to be formed is a chip, it may be advantageous to form the studs on chip before a semiconductor wafer incorporating the chip is diced to separate the individual chips contained in the wafer.

In the present specification "comprise" means "includes or consists of" and "comprising" means "including or consisting of".

The features disclosed in the foregoing description, or the following claims, or the accompanying drawings, expressed in their specific forms or in terms of a means for performing the disclosed function, or a method or process for attaining the disclosed result, as appropriate, may, separately, or in any combination of such features, be utilised for realising the invention in diverse forms thereof.

CLAIMS:

1. A method of constructing an electrical contact on an electronic component, comprising providing a protruding electrically conducting core on the component at a site where an interconnection is to be made, and dipping the core in molten solder, without using a mask, so that the solder adheres to the core and forms a solder bump on the core.

2. A method according to claim 1, comprising forming the electrically conducting core by attaching a metal stud to the component at the site where the interconnection is to be made.

3. A method according to claim 2, comprising attaching the metal stud to a contact pad of the component by wire bonding.

4. A method according to claim 2 or 3, comprising coining the metal stud after it has been formed on the component.

5. A method according to any preceding claim, comprising forming the electrically conducting core from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

6. A method according to any one of claims 2 to 4, comprising forming the metal stud from a length of wire which is bonded to a contact pad of the component and which is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

7. A method according to any preceding claim, comprising forming the solder bump by dipping the electrically conducting core into a bath of molten solder.

8. A method according to any one of claims 1 to 6, comprising forming the solder bump by wave soldering.

9. A method of interconnecting two electronic components, comprising forming an electrical contact by the method of any preceding claim on a contact pad of one of the components and forming a bond between the contact thus formed and a contact pad of the other component.

10. An electronic component having a contact which is formed by the method of any one of claims 1 to 8.

11. An electronic component having a contact which is formed by a protruding electrically conducting core and a solder bump formed on and adhering to the core, in which the core of the contact is a metal stud formed by a length of wire bonded to a contact pad of the component.

12. An electronic component according to claim 11, in which the material of the metal stud is selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

13. An electronic component according to claim 11, in which the wire is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

14. An electronic component according to any one of claims 10 to 13, which component is a semiconductor chip.

15. An electronic component according to any one of claims 10 to 13, which component is a substrate.

16. A electronic components package comprising a semiconductor chip and a mounting substrate, in which one of the chip and the substrate has electrical contacts formed in accordance with any one of claims 1 to 8, and the other of the chip and substrate has contact pads bonded to the contacts by the solder bumps of the contacts.