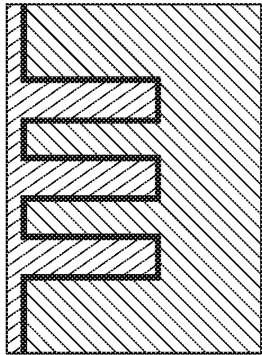


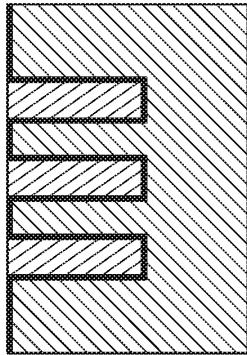
| ATTRIBUTES                                     | SILICON<br>INTERPOSER | EMBEDDED<br>Cu TRACE                       | SAP Cu<br>TRACE                              |
|------------------------------------------------|-----------------------|--------------------------------------------|----------------------------------------------|
| TECHNOLOGY                                     | BEOL                  | POLYMER<br>WITH<br>CONFORMAL<br>SEED METAL | PR +<br>POLYMER<br>WITH BOTTOM<br>SEED METAL |
| PLATFORM                                       | WAFER                 | WAFER                                      | WAFER                                        |
| MAXIMUM<br>ROUTING/mm<br>(L/S: $\mu\text{m}$ ) | ~1300<br>(0.4/0.4)    | ~330<br>(2/1)                              | ~500<br>(1/1)                                |
| COST                                           | HIGH                  | LOW                                        | LOW                                          |
| RF INSERTION<br>LOSS AT HIGH<br>FREQUENCY      | MEDIUM<br>HIGH        | LOW                                        | MEDIUM<br>HIGH                               |

FIG. 1

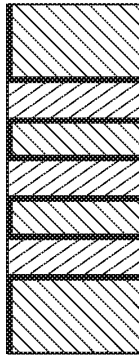
Electroplating  
FIG. 2D



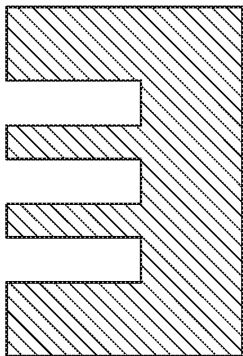
Chemical  
mechanical  
polishing  
FIG. 2E



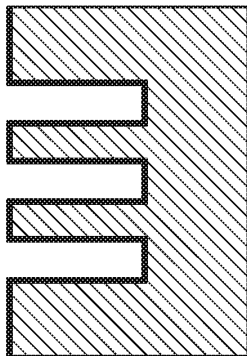
Silicon back  
grinding/etching  
FIG. 2F



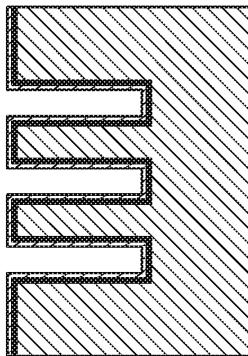
Via etching  
on Silicon  
FIG. 2A



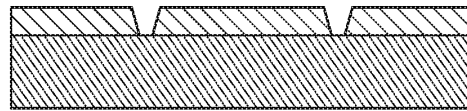
Dielectric layer  
deposition  
FIG. 2B



Barrier/adhesion  
layer and seed  
layer deposition  
FIG. 2C

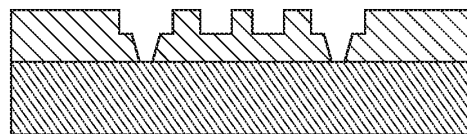


3/5



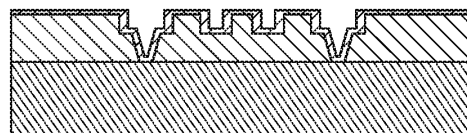
Dielectric1 process

FIG. 3A



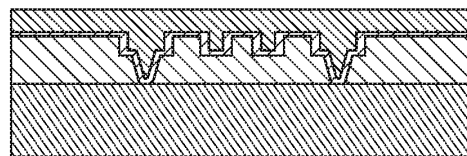
Dielectric2 process

FIG. 3B



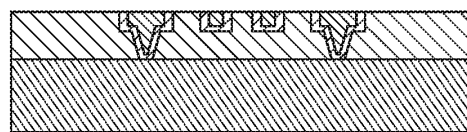
Seed layer PVD

FIG. 3C



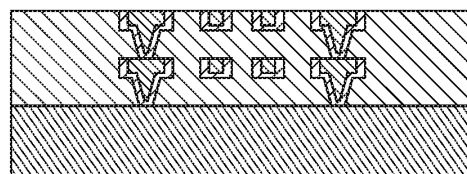
Cu ECP

FIG. 3D



Excess Cu overburden &  
seed layer Removal

FIG. 3E



RDL2 formation

FIG. 3F

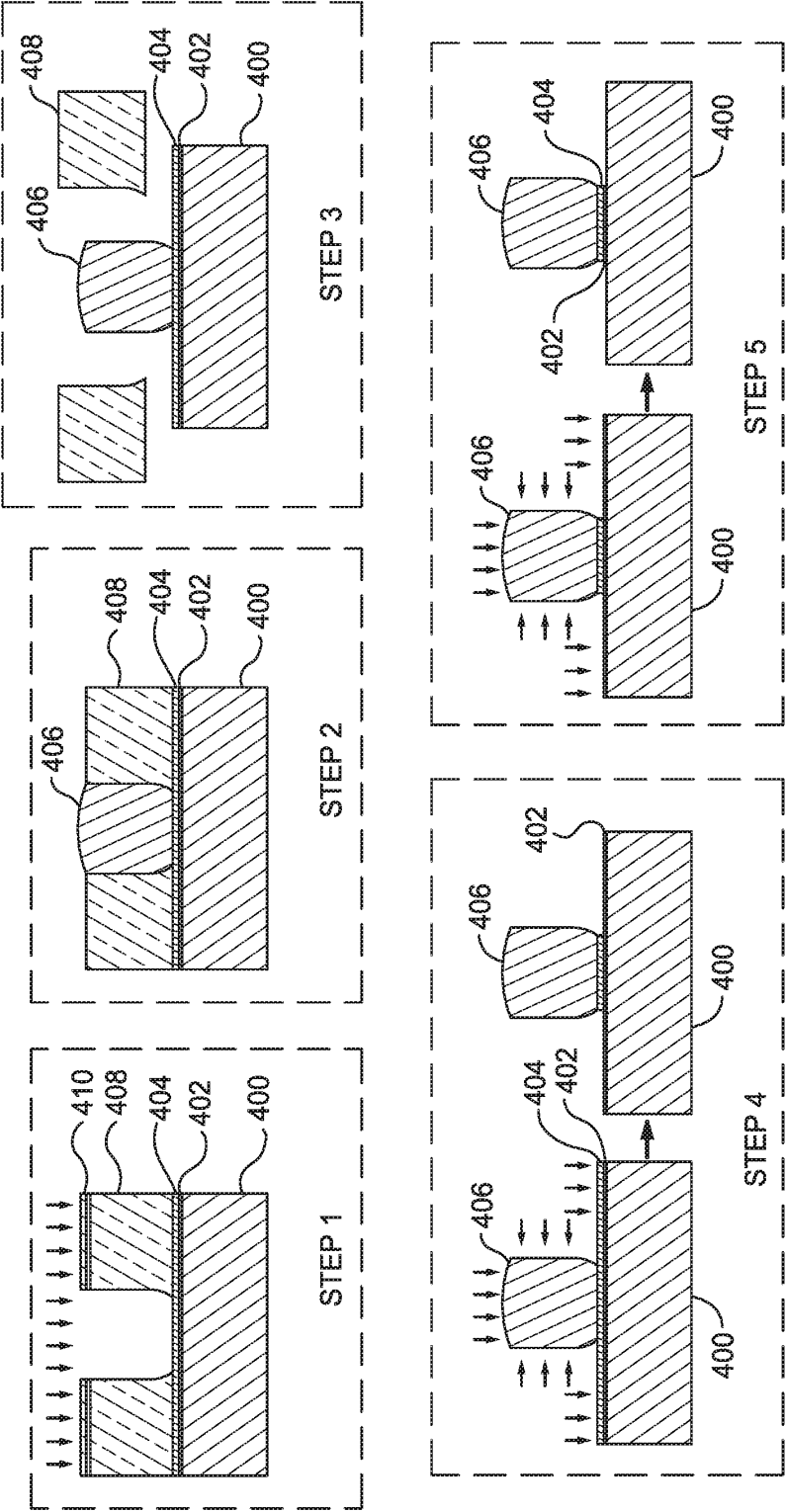


FIG. 4

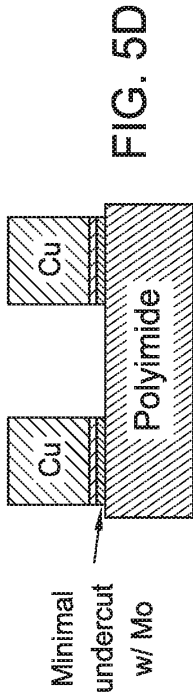


FIG. 5D

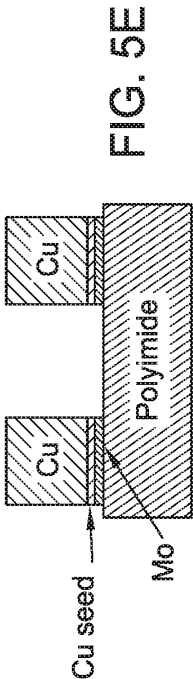


FIG. 5E

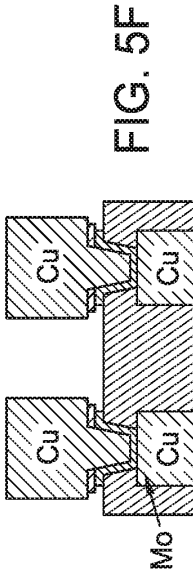


FIG. 5F

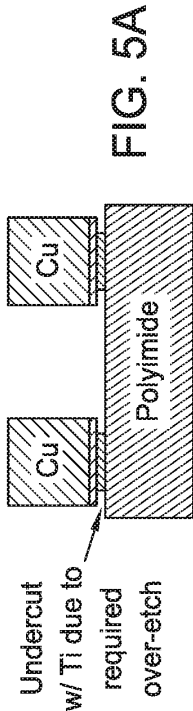


FIG. 5A

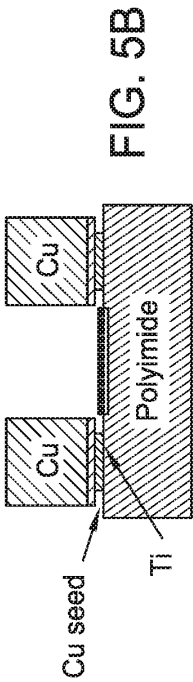


FIG. 5B

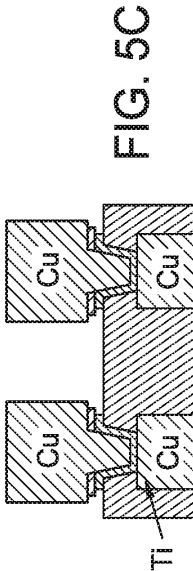


FIG. 5C