

METHOD OF FABRICATING STRAINED CHANNEL DEVICES

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices such as metal oxide semiconductor field effect (MOSFET) devices, and more specifically to devices formed with strained channel regions.

(2) Description of Prior Art

Enhanced performance of MOSFET devices has been addressed via device channel regions formed in strained layers. Increased carrier mobility and thus enhanced device performance has been achieved in both P channel (PMOS) as well as N channel (NMOS) structures via formation of channel regions in strained layers. Formation of strained layers such as a strained silicon layer can be accomplished by formation of the silicon layer on an underlying substrate or layer comprised of silicon - germanium or silicon - germanium carbon.

The magnitude of strain as well as the type of strain, tensile or compressive, is a function of the level of germanium in the underlying materials. To achieve the desired properties of the strained layer the underlying material, such as a silicon - germanium layer or alike substrate, has to remain stable and undisturbed during subsequent device processing, therefore the integration

of the silicon - germanium layer or alike substrate into a MOSFET device process sequence has to be carefully implemented.

The present invention will describe process integration sequences in which the critical silicon - germanium material layer is not adversely effected by subsequent MOSFET processing steps such as formation of shallow trench isolation (STI) elements, or high temperature anneal procedures. Prior art such as Chiu et al in U.S. Pat. No. 2004/0209437 A1, Koester et al in U.S. Pat. No. 2004/0164373 A1, Ngo et al in U.S. Pat. No. 2004/0137742 A1, Wang et al in U.S. Pat. No. 2004/0180509 A1, as well as Comfort et al in U.S. Pat. No. 5,308,785, describe methods of forming isolation structures in strained silicon and in underlying silicon - germanium layers. The above prior art however does not teach the process integration sequence of the present invention in which specific process sequences such as STI formation are integrated into a MOSFET process without adverse consequence of the strained and underlying layers.

SUMMARY OF THE INVENTION

It is an object of this invention to form a MOSFET device featuring a channel region incorporated in a strained layer.

It is another object of this invention to form the strained layer and the underlying silicon - germanium bodies only after formation of STI structures..

It is still another object of this invention to form the underlying silicon - germanium bodies via batch deposition and oxidation procedures applied to an overlying silicon - germanium layer, followed by a selective epitaxial growth of the strained layer.

It is another object of this invention to allow formation of silicon - germanium (Si-Ge) in selective areas only, so hybrid structures for different circuit applications can be formed and integrated in the same wafer.

It is yet another object of this invention to form a complimentary metal oxide semiconductor (CMOS) device via formation of a tensile strained layer for a NMOS device, and of a compressive strained layer for a PMOS device.

It is yet a further object of this invention to optimize NMOS as well as PMOS devices in surface - Channel operating mode thus to achieve better Channel Electrostatic Control to minimize short channel effects.

In accordance with the present invention methods of forming strained layers for a MOSFET device in which the strained layers and overlying silicon - germanium layers are obtained after formation of specific device features such as STI, are described. A shallow trench isolation area is first defined by a composite layer of silicon nitride - silicon oxide, and in a top portion of either a silicon substrate or in a top portion of a Silicon on Oxide (SOI) substrate. Subsequent to patterning of silicon - nitride, silicon oxide, etching into then exposed silicon region, and formation of a silicon oxide liner layer on exposed silicon surfaces (e.g. sidewall,

bottom, and top corners of future Si active areas), the desired STI structure is formed via insulator fill and chemical mechanical polishing (CMP) procedures. Silicon nitride removal and surface cleaning is followed by deposition or sputtering of a polycrystalline silicon - germanium layer. A first embodiment of this invention features an oxidation procedure in which germanium is segregated into the underlying silicon body resulting in the desired silicon - germanium body to be used to accommodate a subsequent overlying strained Silicon layer. Removal of the oxidized material exposes the now formed underlying silicon - germanium crystalline ($\text{Si}_{1-x}\text{Ge}_x$) body wherein x is the weight percent of germanium in the $\text{Si}_{1-x}\text{Ge}_x$ layer. The desired strained silicon layer is next achieved via a selective epitaxial growth (SEG) procedure formed on the underlying exposed $\text{Si}_{1-x}\text{Ge}_x$ body.

A second embodiment of this invention features the formation of both tensile strained silicon - germanium and compressively strained silicon - germanium for the same MOSFET device. After deposition or sputtering of a polycrystalline silicon - germanium layer, photolithographic and dry etching procedures are used to thin a portion of the polycrystalline silicon germanium layer in a region of the MOSFET device to be used for P channel device fabrication. A subsequent oxidation procedure results in germanium segregation into the underlying silicon body with a greater level of germanium incorporated into the portion of silicon body underlying the unetched or thicker polycrystalline silicon - germanium layer, when compared to level of germanium incorporated into the portion of silicon body underlying the thinner polycrystalline silicon - germanium layer. Removal of oxidized material followed by SEG of a thin silicon - germanium layer, with the chosen [Ge] concentration between the two

underlying substrates concentration, will result in a silicon - germanium layer featuring tensile strain overlying the silicon - germanium body with the greater germanium incorporation while a compressively strained silicon - germanium layer is grown on the silicon body having the lower germanium concentration. The top layers for all regions will be designated as SiGe_z while SiGe_x and SiGe_y will be the two underlying layers, z chosen to be $x < z < y$. Subsequent MOSFET processing such as gate insulator growth, conductive gate structure formation, source/drain formation, result in a MOSFET device featuring either PMOS, NMOS or CMOS devices.

A third iteration of this invention features the growth of a thin silicon layer on underlying layers SiGe_x and SiGe_y , with the silicon layer featuring tensile strain overlying the silicon - germanium body (SiGe_y) with greater germanium incorporation while a compressively strained silicon - germanium layer is grown on the silicon - germanium body (SiGe_x) having the lower germanium concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 10, which schematically in cross-sectional style show key stages of fabrication for either a tensile or compressive strained silicon layer on an underlying silicon -germanium body, formed after STI formation.

Figs. 11 - 14, which schematically in cross-sectional style show key stages for integration of both tensile and compressive strained layers on a underlying silicon - germanium body, again formed after STI formation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of forming strained silicon layers on an underlying silicon - germanium body for incorporation of MOSFET channel regions, wherein the strained silicon regions and underlying silicon - germanium body were formed after formation of specific device features such as shallow trench isolation (STI) structures, will now be described in detail. Semiconductor substrate 1, shown schematically in Fig. 1, is comprised of single crystalline, P type silicon, featuring a <100> crystallographic orientation. The substrate orientation is not critical for this invention and thus can be any orientation if desired without detracting from the spirit of this invention. If desired a silicon on oxide (SOI) layer 2a, can be formed on semiconductor substrate 1, to reduce capacitance and enhance performance of subsequently formed devices. This invention will be described using the SOI option with silicon layer 2a, at a thickness between about 100 Angstroms to 0.5 μm , (100 Angstroms will be called an ultra-thin body and will be a fully depleted body while SOI at a thickness of about 0.5 μm will be a partially depleted body). Layer 1, can also be a buried oxide layer for example with a thickness between about 1000 Angstroms to 1 μm . Not shown in the drawings are N well and P well regions formed in SOI layer 2a, to accommodate the PMOS and NMOS devices. The well regions can be intrinsic or doped, with doped regions formed via ion implantation of specific ions such as

boron, arsenic phosphorous, indium, or antimony, followed by high temperature annealing to activate the implanted ions. It is imperative to form the well regions prior to forming the strained silicon and underlying silicon - germanium bodies since the high temperature processes of well formation would result in unwanted out gassing of germanium from a silicon - germanium materials.

Formation of a shallow trench isolation (STI) structure is next addressed and schematically shown using Figs. 2 - 6. The process steps, dry etching, liner formation, etc, could again deleteriously influence the integrity of a strained silicon layer as well as an underlying silicon - germanium body, therefore the STI structure is formed prior to formation of these layers. Silicon oxide layer 3, to be used as a pad oxide, is first obtained at a thickness between about 50 to 150 Angstroms, preferably at 100 Angstroms, via thermal oxidation procedures. This is followed by deposition of silicon nitride layer 4, at a thickness between about 500 to 1500 Angstroms, preferably at 1000 Angstroms, via low pressure chemical vapor deposition (LPCVD) or via plasma enhanced chemical vapor deposition (PECVD) procedures. The use of an anti-reflective coating film overlying silicon nitride layer 4, prior to photolithographic processing is optional. Photolithographic and selective anisotropic reactive ion etching (RIE) procedures, are then applied to define shallow trench shape 20, in silicon nitride layer 4, in silicon oxide layer 3, and in the entire or in a top portion of SOI layer 2a. This is schematically shown in Fig. 2. The anisotropic RIE procedure is performed using Cl_2 or CF_4 as an etchant for silicon nitride, CHF_3 as an etchant for silicon oxide, and Cl_2 or SF_6 as an etchant for silicon, and the chemistry or mixed chemistry chosen for etching of each layer is not limited to the above. Shallow trench

shape 20, is formed in the entire thickness of SOI layer 2a, to a depth between about 100 to 3500 Angstroms. (For a body thickness <3500 Angstroms the depth is all reach through, for >3500 Angstroms in body thickness the thickness of 3500 Angstroms is fixed, just like the formation in the bulk silicon. If desired shallow trench shape 20, can be formed only in top portion of SOI layer 2a, terminating in a bottom portion of SOI layer 2a).

With a photoresist shape (not shown in te drawings) used to define shallow trench shape 20, still in place lateral pullback 5, of exposed portions of silicon nitride layer 4, is performed. This is accomplished via an isotropic dry etch procedure using Cl_2 or CF_4 as an etchant, or via a wet etch procedure using hot phosphoric acid as an etchant for silicon nitride. Pullback 5, shown schematically in Fig. 3, is between about 100 to 200 Angstroms. Removal of the shallow trench defining photoresist shape is now accomplished via plasma oxygen ashing procedures followed by wet clean procedures. A buffered hydrofluoric acid component used in the wet clean procedure results in removal of portions of silicon oxide layer 3, exposed after the silicon nitride pullback procedure resulting in an additional silicon oxide pull back of between about 100 to 200 Angstroms silicon nitride layer 4. The result of these procedures is schematically shown in Fig. 3.

To repair the etched trench sidewall surfaces and also protect exposed surfaces of SOI layer 2a, from a subsequent chemically deposited insulator layer used to fill shallow trench shape 20, liner layer 6, is formed to a thickness between about 100 to 400 Angstroms, preferably at 200 Angstroms. Liner layer 6, shown schematically in Fig. 4, is comprised of silicon dioxide

formed via a thermal oxidation procedure performed at a temperature between about 900 to 1200°C, preferably at 1100° C. The thickness of silicon dioxide liner layer 6, is optimized to satisfy the corner rounding required by the subsequently formed devices. Silicon - germanium layers if exposed to the above high temperature oxidation procedure would be deleteriously altered as a result of germanium out gassing, and poor silicon - germanium oxide quality.

Insulator layer 7a, comprised of silicon oxide is next deposited via LPCVD, PECVD or via (HDP) high density plasma deposition procedures to a thickness between about 5000 to 8000 Angstroms, completely filling shallow trench shape 20. Removal of unwanted portions of silicon oxide layer 7a, from the top surface of silicon nitride layer 4, is accomplished via a CMP procedure for better planarized surface. If desired a RIE procedure can be employed using CHF_3 as a selective etchant for silicon oxide layer 7a, with the selective RIE procedure terminating at the appearance of the top surface of silicon nitride layer 4. This is schematically shown in Fig. 5. Silicon nitride layer 4, is next selectively removed preferably via a hot phosphoric acid treatment resulting in the silicon oxide filled shallow trench opening shown schematically in Fig. 6. Alternately a selective RIE procedure may be utilized.

Careful wet clean procedures using BHF as a component are next employed to prepare exposed surfaces of SOI layer 2a, for deposition of $\text{Si}_{1-x}\text{Ge}_x$ layer 8. $\text{Si}_{1-x}\text{Ge}_x$ layer 8, wherein x is the weight percent of germanium, can be obtained via a low temperature chemical vapor deposition (LPCVD) procedure using the identical apparatus used for polysilicon deposition. The LPCVD procedure is performed at a temperature between about 500 to 700° C, preferably at

600°C, using silane or disilane as a source for the silicon component of $\text{Si}_{1-x}\text{Ge}_x$ layer 8, while germane is employed as a source for the germanium component. Germanium weight percent x , is adjusted via flow rate levels of silane and germane. $\text{Si}_{1-x}\text{Ge}_x$ layer 8, shown schematically in Fig. 7, is deposited to a thickness between about 500 to 1500 Angstroms, preferably at 1000 Angstroms, with a germanium weight percent between about 10% to 70%. If desired $\text{Si}_{1-x}\text{Ge}_x$ layer 8, can be obtained via d.c. or r.f. sputtering procedures, for this case a target comprised with only a specific percent of silicon and of germanium can be employed. Alternately, silicon epitaxial growth (SEG) could be used to form $\text{Si}_{1-x}\text{Ge}_x$ layer 8.

A critical oxidation procedure is next performed in an oxygen - steam ambient at a temperature between about 900 to 1100° C. This temperature is selected to be less than the melting point of $\text{Si}_{1-x}\text{Ge}_x$, wherein the melting point decreases with increasing x . The oxidation procedure in addition to converting the silicon component of $\text{Si}_{1-x}\text{Ge}_x$ layer 8, to silicon oxide layer 18, also allows segregation of germanium into the underlying SOI layer to result. The resulting underlying SOI layer is now single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b, comprised with a weight percent of germanium between about 10% up to >90 %. This is schematically shown in Fig. 8. Selective removal of silicon oxide layer 18, is next accomplished via a wet BHF procedure, also may resulting in a thinner silicon oxide component 7b, filling the shallow trench shape. This is schematically shown in Fig. 9. Single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b, comprised with a desired germanium weight content is now in the correct form to allow growth of an overlying strained silicon layer to proceed.

A selective epitaxial growth (SEG) procedure is next employed to grow single crystalline silicon or silicon - germanium layer 9, on exposed top surfaces of single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b. The SEG procedure is performed at a temperature between about 500 to 700° C, preferably at 600 to 650°C, using silane or disilane for the silicon option, while adding germane for a silicon - germanium option. Single crystalline silicon layer 9, shown schematically in Fig. 10, is selectively grown at a thickness between about 50 to 200 Angstroms, preferably at 100 Angstroms as channel thickness demands, only on exposed top surfaces of single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b. The ability to grow the above layer on underlying single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b, results in a tensile strained silicon layer 9. The magnitude of tensile strain is a function of the weight percent of germanium in underlying single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b. Strained silicon layer 9, will now be used to accommodate a MOSFET channel region with enhanced carrier mobility thus resulting in enhanced MOSFET performance. The MOSFET device is completed via: formation of a gate insulator layer on strained silicon layer 9; depositing and definition of a conductive gate structure on the underlying gate insulator layer; and formation of a source/drain region in regions of strained silicon layer 9, not covered by the conductive gate structure.

A second embodiment of this invention teaches a process which allows a first portion of a silicon - germanium layer to be selectively formed with tensile strain while a second portion of the same selectively grown silicon - germanium layer is formed with compressive strain. Referring to Fig. 11, with the insulator filled STI structure in place Si and using the structure of Fig. 6 as a starting point, $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, is deposited wherein x is the weight percent of

germanium. $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, can again be obtained via a low temperature chemical vapor deposition (LPCVD) procedure using the identical apparatus used for polysilicon deposition. The LPCVD procedure is performed at a temperature between about 500 to 700°C, using silane or disilane as a source for the silicon component of $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, while using germane as a source for the germanium component. Germanium weight percent x , is adjusted via flow rate levels of silane and germane. $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, is deposited to a thickness between about 500 to 1500 Angstroms, preferably at 1000 Angstroms, with a germanium weight percent between about 10% to 70%. If desired $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, can be obtained via d.c. or r.f. sputtering procedures. Photoresist shape 11, is next formed and used as an etch mask to allow removal or partial removal of a top portion of $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, to be performed. A RIE procedure employed using Cl_2 or SF_6 as an etchant results in the attainment of thinner $\text{Si}_{1-x}\text{Ge}_x$ layer 10b, now at a thickness between about 0 to 500 Angstroms, overlying a second portion of SOI layer 2a. Unetched portions of $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, at a thickness between about 500 to 1500 Angstroms remain overlying a first portion of SOI layer 2a. An option for a hybrid structure is the thinning of layer 10a, to where the thickness of layer 10b, is 0 Angstroms (i.e., total removal), resulting in no germanium entering underlying region 2a. This could be used for the subsequent formation of, for example, leakage sensitive devices or the like.

After removal of photoresist shape 11, via plasma oxygen ashing and wet clean procedures a critical oxidation procedure is performed in an oxygen - steam ambient at a temperature between about 900 to 1000°C. The oxidation procedure is employed to completely convert the unetched $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, to silicon oxide layer 20a, and to completely convert thinner $\text{Si}_{1-x}\text{Ge}_x$

layer 10b, to silicon oxide layer 20b. The oxidation procedure again results in segregation of germanium into underlying SOI layer 2a. The extent of Ge segregation into the underlying SOI layer 2a, is a function of the thickness or amount of germanium in the overlying pre-oxidized $\text{Si}_{1-x}\text{Ge}_x$ layer. Since $\text{Si}_{1-x}\text{Ge}_x$ layer 10b, is thinner than the unetched $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, less germanium segregation into the underlying SOI layer occurs when compared to the level of germanium segregation into the portion of SOI layer 2a, underlying $\text{Si}_{1-x}\text{Ge}_x$ layer 10a with full as-deposited thickness. The oxidation procedure of $\text{Si}_{1-x}\text{Ge}_x$ layer 10a, at a pre-oxidized thickness between about 600 to 800 Angstroms, (with [Ge] at 50% as an example), allows germanium segregation to occur in underlying single crystalline body $\text{Si}_{1-x}\text{Ge}_x$ 2b, wherein x the weight percent of germanium in single crystalline body $\text{Si}_{1-x}\text{Ge}_x$ layer 2b, is between about 60 to 80 percent, resulting in a final thickness of about 500 Angstroms. The same oxidation procedure applied to thinner $\text{Si}_{1-x}\text{Ge}_x$ layer 10b, results in single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2c, wherein the weight percent of germanium is only between about 20% to 40%. This is schematically shown in Fig. 12.

Selective removal of silicon oxide layer 20a, and of 20b, is next accomplished via a wet BHF procedure. This procedure also results in thinning of the silicon oxide shape of the STI structure resulting in thinner silicon oxide component 7b. This is schematically shown in Fig. 13. The selective epitaxial growth (SEG) procedure previously described in this first embodiment of this invention is again employed to grow single crystalline silicon-germanium layers on exposed top surfaces of single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body 2b, and $\text{Si}_{1-x}\text{Ge}_x$ body 2c. The SEG procedure is performed at a temperature between about 500 to 700°C, preferably at 600°C. The silicon-

germanium layer is achieved via the addition of germane to either a silane or disilane flow. Single crystalline silicon - germanium ($\text{Si}_{1-z}\text{Ge}_z$) layer 12a, at a thickness between about 50 to 200 Angstroms (thinner than the underlying substrate), preferably at 100 Angstroms, is selectively grown on underlying $\text{Si}_{1-x}\text{Ge}_x$ body 2b, and is comprised with a tensile strain. The tensile strain featured in single crystalline silicon - germanium layer 12a, is achieved via selective epitaxial growth on an underlying $\text{Si}_{1-x}\text{Ge}_x$ body 2b, comprised with a germanium weight percent between about 60% to 80%. The tensile strain of single crystalline silicon layer 12a, will allow enhancement of electron mobility to be realized thus enhancing the performance of subsequently fabricated NMOS devices. The same SEG procedure results in the selective growth of single crystalline silicon-germanium($\text{Si}_{1-z}\text{Ge}_z$) layer 12b, on underlying $\text{Si}_{1-x}\text{Ge}_x$ body 2c. However single crystalline silicon - germanium layer 12b, is comprised with compressive strain as a result of growth on underlying $\text{Si}_{1-x}\text{Ge}_x$ body 2c, which is comprised with a lower germanium weight percent between about 20 to 40 weight percent, than counterpart $\text{Si}_{1-x}\text{Ge}_x$ body 2b, because $x < z$. The compressive nature of single crystalline silicon - germanium layer 12b, will allow enhancement of hole mobility to be realized thus enhancing the performance of subsequently fabricated PMOS devices. The result of the SEG procedure is schematically shown in Fig. 14.

A third embodiment of this invention features the growth of a single crystalline layer ($\text{Si}_{1-z}\text{Ge}_z$) 12a or 12b, on underlying layers $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-y}\text{Ge}_y$, wherein the germanium content [z] is zero weight percent. Silicon layer 12a, featuring tensile strain is grown overlying the silicon-germanium body ($\text{Si}_{1-y}\text{Ge}_y$) comprised with the greater germanium incorporation, while

compressively strained silicon layer 12b is grown on the silicon-germanium body ($\text{Si}_{1-x}\text{Ge}_x$) having the lower germanium concentration.

Complimentary metal oxide semiconductor (CMOS) devices can now be formed wherein NMOS devices can be formed in with enhanced electron mobility in single crystalline silicon layer 12a, while counterpart PMOS devices can be formed with enhanced hole mobility in single crystalline silicon layer 12b. The completion of the CMOS devices feature: gate insulator layer formed on both single crystalline silicon layer 12a and 12b; definition of a conductive gate structure on the underlying gate insulator layer; and formation of an N type and P type source/drain region in regions of the strained silicon layers not covered by the conductive gate structure. The ability to form the $\text{Si}_{1-x}\text{Ge}_x$ bodies and the overlying strained silicon layers after STI formation and after high temperature processing did not allow the integrity of the above layers to be degraded.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is:

1. A method of forming a strained semiconductor layer for a metal oxide

semiconductor field effect transistor (MOSFET) device, comprising the steps of:

providing a single crystalline semiconductor body;

forming an insulator filled, shallow trench isolation (STI) structure in a top portion

5 of said single crystalline semiconductor body;

forming a semiconductor alloy layer;

performing an oxidation procedure to convert said semiconductor alloy layer to an
insulator layer and segregating a portion of a metal component of said semiconductor
alloy layer into a top portion of said single crystalline semiconductor body resulting in

10 formation of a single crystalline semiconductor alloy body;

removing said insulator layer; and

growing said strained semiconductor layer on said single crystalline semiconductor
alloy body.

2. The method of claim 1, wherein said single crystalline semiconductor body is a

15 single crystalline silicon substrate, comprised with a <100> crystallographic
orientation.

3. The method of claim 1, wherein said single crystalline semiconductor body is a
silicon on insulator (SOI) layer, wherein the thickness of said SOI layer is between
about 100 Angstroms to 0.5 um.

4. The method of claim 1, wherein said insulator filled, STI structure is a silicon oxide filled STI structure, wherein the depth of said STI structure in said single crystalline semiconductor body is between about 100 to 3500 Angstroms.
5. The method of claim 1, wherein said semiconductor alloy layer is a silicon - germanium ($\text{Si}_{1-x}\text{Ge}_x$) layer, wherein x is the content of germanium in $\text{Si}_{1-x}\text{Ge}_x$, between about 10 to 70 weight percent.
6. The method of claim 1, wherein said semiconductor alloy layer is obtained at a thickness between about 500 to 1500 Angstroms via chemical vapor deposition procedures such as a low temperature chemical vapor deposition (LPCVD) procedure.
- 10 7. The method of claim 1, wherein said semiconductor alloy layer is obtained at a thickness between about 500 to 1500 Angstroms via sputtering procedures.
8. The method of claim 1, wherein said oxidation procedure is a thermal oxidation procedure performed at a temperature between about 900 to 1100°C, in an oxygen - steam ambient.
- 15 9. The method of claim 1, wherein said single crystalline semiconductor body is a single crystalline silicon - germanium ($\text{Si}_{1-x}\text{Ge}_x$) body, comprised with a germanium content between about 20 to 80 weight percent.

10. The method of claim 1, wherein said strained semiconductor layer is a single crystalline silicon layer obtained via selective epitaxial growth (SEG) procedures to a thickness between about 50 to 200 Angstroms.

11. The method of claim 1, wherein said strained semiconductor layer is comprised of tensile strain.

12. A method of integrating the formation of a tensile strained silicon layer and of a compressive strained silicon layer on underlying semiconductor alloy bodies, performed after formation of insulator filled, shallow trench isolation (STI) structures, comprising the steps of:

providing a single crystalline silicon body;

forming said insulator filled, STI structure in a top portion of said single crystalline silicon body;

depositing a silicon - germanium ($\text{Si}_{1-x}\text{Ge}_x$) layer;

performing a patterning procedure to thin a second portion of said $\text{Si}_{1-x}\text{Ge}_x$ layer in a region in which said second portion of said $\text{Si}_{1-x}\text{Ge}_x$ layer overlays a second portion of said single crystalline silicon body, while a first portion of said $\text{Si}_{1-x}\text{Ge}_x$ layer located overlying a first portion of said single crystalline silicon body remains unetched;

performing an oxidation procedure to convert the unetched first portion of said $\text{Si}_{1-x}\text{Ge}_x$ layer and thinned second portion of said $\text{Si}_{1-x}\text{Ge}_x$ layer to silicon oxide,

- 15 converting said first single crystalline silicon body to a first single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body comprised with a first weight percent of germanium, and converting said second single crystalline silicon body to a second single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body comprised with a second weight percent of germanium;
- removing said silicon oxide layer; and
- selectively forming said tensile strained silicon layer on said first single crystalline $\text{Si}_{1-x}\text{Ge}_x$ layer and forming said compressive strained silicon layer on said second single crystalline $\text{Si}_{1-x}\text{Ge}_x$ layer.
13. The method of claim 12, wherein said single crystalline semiconductor body is a
5 single crystalline silicon substrate comprised with a <100> crystallographic orientation.
14. The method of claim 12, wherein said single crystalline semiconductor body is a silicon on insulator (SOI) layer, wherein the thickness of said SOI layer is between about 100 Angstroms to 0.5 μm .
15. The method of claim 12, wherein said insulator filled, STI structure is a silicon
10 oxide filled STI structure, wherein the depth of said STI structure in said single crystalline semiconductor body is between about 100 to 3500 Angstroms.
16. The method of claim 12, wherein said silicon - germanium ($\text{Si}_{1-x}\text{Ge}_x$) layer, wherein x is the content of germanium in $\text{Si}_{1-x}\text{Ge}_x$, is comprised with a weight percent of germanium between about 10 to 70.

- 15 17. The method of claim 12, wherein said $\text{Si}_{1-x}\text{Ge}_x$ layer is obtained at a thickness between about 500 to 1500 Angstroms via chemical vapor deposition procedures such as a low temperature chemical vapor deposition (LPCVD) procedure.
18. The method of claim 12, wherein said $\text{Si}_{1-x}\text{Ge}_x$ layer is obtained at a thickness between about 500 to 1500 Angstroms via sputtering procedures.
19. The method of claim 12, wherein said patterning procedure is performed using a reactive ion etching (RIE) procedure employed using Cl_2 or SF_6 as an etchant.
- 5 20. The method of claim 12, wherein the thickness of said thin second portion of said $\text{Si}_{1-x}\text{Ge}_x$ layer is between about 0 to 500 Angstroms.
21. The method of claim 12, wherein said oxidation procedure is a thermal oxidation procedure performed at a temperature between about 900 to 1100°C, in an oxygen - steam ambient.
- 10 22. The method of claim 12, wherein said first single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body is comprised with said first weight percent of germanium between about 60% to 80%.
23. The method of claim 12, wherein said second single crystalline $\text{Si}_{1-x}\text{Ge}_x$ body is comprised with said second weight percent of germanium between about 20% to 40%.
24. The method of claim 12, wherein strained silicon layers are single crystalline

15 silicon layers obtained via selective epitaxial growth (SEG) procedures to a thickness between about 50 to 200 Angstroms.

25. The method of claim 12, wherein a strained semiconductor layer is comprised of tensile strain.

26. The method of claim 12, wherein a strained semiconductor layer is comprised of compressive strain.

27. A complimentary metal oxide semiconductor (CMOS) structure on a semiconductor substrate, comprising:

a silicon on insulator (SOI) layer on said semiconductor substrate;

a first portion of said SOI layer comprised with a first concentration of an element;

5 a second portion of said SOI layer comprised with a second concentration of said element, wherein said first concentration of said element in said first portion of said SOI layer is greater than said second concentration of said element in said second portion of said SOI layer;

10 a first portion of a strained semiconductor layer comprised with a first strain, located on said first portion of said SOI layer, and a second portion of a strained semiconductor layer comprised with a second strain, located on said second portion of said SOI layer;

a gate insulator layer on said first portion and on said second portion of said semiconductor layer;

a first conductive gate structure on a first portion of said gate insulator layer which

15 in turn is located on said first portion of said semiconductor layer, and a second
conductive gate structure located on a second portion of said gate insulator layer which
in turn is located on said second portion of said semiconductor layer;

a first source/drain region of a first conductivity type located in a portion of said
first portion of said semiconductor layer not covered by said first conductive gate, and
20 a second source/drain region of a second conductivity type located in a second portion
of said semiconductor layer not covered by said second conductive gate structure; and

an insulator filled shallow trench structure located between said first portion of said
semiconductor layer and said second portion of said semiconductor layer, extending
through said semiconductor layer and through said SOI layer.

28. The CMOS structure of claim 27, wherein the thickness of said silicon on insulator
5 layer is between about 100 Angstroms to 0.5 μm .

29. The CMOS structure of claim 27, wherein said element in said SOI layer is
germanium

30. The CMOS structure of claim 27, wherein said first concentration of said element
in said first portion of said SOI layer is between about 60 to 80 weight percent.

10 31. The CMOS structure of claim 27, wherein said second concentration of said element
in said second portion of said SOI layer is between about 20 to 40 weight percent.

32. The CMOS structure of claim 27, wherein said strained semiconductor layer is a silicon layer at a thickness between about 50 to 200 Angstroms.
33. The CMOS structure of claim 27, wherein said strained semiconductor layer is a
15 silicon -germanium alloy layer at a thickness between about 50 to 200 Angstroms.
34. The CMOS structure of claim 27, wherein said first strain of said first portion of said semiconductor layer is a tensile strain.
35. The CMOS structure of claim 27, wherein said second strain of said second portion of said semiconductor layer is a compressive strain.