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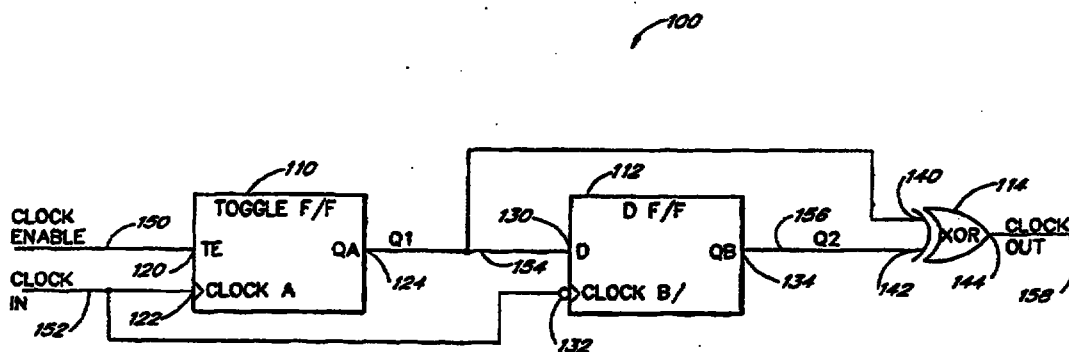


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(54) Title: GLITCH-FREE CLOCK ENABLE CIRCUIT



(57) Abstract

A circuit (100) utilizes a toggle flip-flop (110), a D flip-flop (112) and combinational logic (114) to generate a clock signal (158) which can be enabled or disabled without creating spikes or shortened pulses in the clock signal. The circuit receives an input clock signal (152) and an input clock enable signal (150). The circuit (100) generates an output clock signal (158) which is an enabled/disabled version of the input clock signal (152), controlled by the input clock enable signal (150). The circuit (100) thus provides the operational advantages of enabling or disabling, with a single control signal, groups of logic circuits triggered by a common clock signal.