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SPECIFICATION

TITLE OF THE INVENTION

Semiconductor device and manufacturing method thereof

BACKGROUND OF THE INVENTION

The present invention concerns a semiconductor integrated circuit device technique and, more in particular, it relates to a useful technique to be applied to portable equipments such as portable telephones and handy type personal computers, for which a trend of reducing the size, the weight and the thickness has become vigorous.

Recently, a trend of reducing the size, the weight and the thickness has become vigorous for electronic equipments along with improved function and performance for them. This is greatly due to rapid increase of personal equipments such as personal telephones or handy type personal computers in recent years. Further, man-machine interface functions are increased in personally manipulated equipments, for which easy handlability and operability have been considered important more and more. It is considered that the trend will become more and more conspicuous in expected regular multimedia are.

Under such a circumstance, development for increasing the density and the integration degree of semiconductor

chips have been made continuously, in which the side and the number of electrodes for the semiconductor chips have been increased, while the size of the packages has been increased rapidly. Accordingly, narrowing for the pitch of terminal leads has been promoted for proceeding the size reduction of the packages, and while makes mounting of the package difficult abruptly.

In view of the above, it has been proposed in recent years high density packages with supermultiple pins having the same area as that of the semiconductor chips and package techniques can be mentioned, for example, as described in literatures such as "Nikkei Microdevice" p 98 - p 102, issued on May 1, 1994, "Nikkei Microdevice" p 96 - p 97, issued on February 1, 1995 by Nikkei BPCO and "Electronic Material", p 22 - p 28, issued on April 1, 1995 (Heisei 7) by Kogyo Chosakai. One example of the structures in such package techniques, for example, as described in Fig. 6 of the "Electronic Material", has a package structure in which a flexible wiring substrate is disposed by way of an elastomer (elastic material) on the surface of a semiconductor chip, leads on one end of wirings of the flexible wiring substrate are electrically connected with bonding pads on the surface of the semiconductor chip, and bump lands on the other end of the wirings of the flexible wiring substrate are electrically connected with the solder bumps.

The package structure has an outer size about equal with or greater than that of a semiconductor chip by the size of a protection frame optionally attached to the periphery of the chip, for which a flexible wiring substrate formed with solder bumps is used. The wiring pattern of the wiring substrate is made of a Cu foil applied with Au plating on one side, the top ends of which to be connected with the pad of the chip constitute a lead pattern only composed of Au by the etching for the Cu foil. In this structure, the flexible wiring substrate is bonded by an elastomer on the surface of the semiconductor chip and then the Au leads are connected with the bonding pads of the semiconductor chip.

SUMMARY OF THE INVENTION

By the way, according to the study made by the present inventor on the package structure as described above, the following problems are considered. For example, since the flexible wiring substrate in the package structure described above has such a structure typically represented by TCP (Tape Carrier Package) in which a Cu wiring pattern is formed on the surface of a polyimide tape, and an elastomer is formed to the wiring substrate on the side of the wiring surface, it is difficult to mount the elastomer uniformly and stably because of unevenness of the wiring pattern on the flexible wiring substrate. That is, it may be considered

such problems that voids not filled with the elastomer are formed near both sides of protrusions of the wiring pattern upon coating or appending the elastomer on the flexible wiring substrate and the step of bonding the semiconductor chip can not be conducted stably since the size and the shape of the elastomer are not stable.

Further, bump electrodes are formed to the wiring substrate on the side of the tape. That is, the bump electrode is connected with the wirings by way of a through hole formed to the tape. Since the thickness of the tape is relatively large, for example, as 50 μm, if the pitch between the bump electrodes is smaller than the thickness of the tape, the aspect ratio of the through hole is increased to bring about a worry that the bump electrode and the wiring are not connected. Accordingly, there may be a worry that increase for the number of pins of the package is restricted.

In view of the above, an object of the present invention is to provide a semiconductor integrated circuit device capable of mounting an elastic structural material to a wiring substrate stably at a high accuracy, and making the bonding step of a semiconductor chip stable thereby enabling assembling at high yield.

Another object of the present invention is to provide a technique of promoting increase for the number of pins in a

package.

An object of the present invention is to provide a semiconductor integrated circuit device capable of obtaining excellent electrical properties in view of noise resistance by the adoption of a multiple wiring layer structure.

An object of the present invention is to prevent wiring from contamination with ingredients of an elastic structural material.

An object of the present invention is to prevent a semiconductor chip from injury, improve the reliability of the semiconductor chip, as well as prevent connection failure between an elastic structural material and the semiconductor chip, worsening of the flatness for the wiring substrate and lowering of reliability.

An object of the present invention is to eliminate requirement for a soft-modified special wire bonder and obtaining an effect of shortening the tact time upon bonding by further simplifying the trace of a bonding tool.

An object of the present invention is to solve a problem upon disconnection of wirings.

An object of the present invention is to reduce damages to passivation or a semiconductor chip therebelow and further improving the bondability by preventing contamination of wirings.

An object of the present invention is to increase a

bonding strength between wirings and a substrate material and obtaining a stable notch cutting performance.

An object of the present invention is to suppress warp of a wiring substrate and improve bondability with a bonding material and constitute a package of excellent moisture proofness and reliability.

An object of the present invention is to improve groove-fillage of an elastic structural material, capable of increasing the strength of a metal mask by using a plurality of one side suspending portions and further improving the groove-fillage by the formation of a stopping dam for sealant flow.

An object of the present invention is to improve the bondability and prevent damages to a semiconductor chip in inner lead bonding technique.

An object of the present invention is to form a suitable S-shaped configuration with no return of a bonding tool but by merely driving done the bonding tool vertically by a wiring design considering a bending stress ratio.

An object of the present invention is to reduce occurrence of cracks in wirings per se and moderate bonding damages to a semiconductor chip.

An object of the present invention is to suppress bleeding of low molecular weight ingredients of a elastic structural material and further avoid disadvantage such as

involving of voids upon forming the elastic structural material by surface flattening.

An object of the present invention is to improve a fabrication accuracy for hole diameter for connection of a bump electrode in a method of manufacturing a semiconductor integrated circuit.

An object of the present invention is to constitute a semiconductor package capable of bonding bump electrodes more satisfactorily, reducing the arranging pitch of bump electrodes and having output terminals at a higher density in a method of manufacturing a semiconductor integrated circuit device.

These and other objects, as well as novel features of the present invention will become apparent by reading the descriptions in the specification with reference to the accompanying drawings.

Among the inventions disclosed in the present application, outlines will be explained simply for typical examples as follows.

That is, one of semiconductor integrated circuit devices according to the present invention provides a package structure applied to a semiconductor integrated circuit device in which a wiring substrate is disposed by way of an elastic structural material on a main surface of a semiconductor chip, lead portions on one end of wirings of the wiring

substrate are electrically connected with external terminals on the main surface of the semiconductor chip, and land portions on the other end of the wirings of the wiring substrate are electrically connected with bump electrodes, wherein the wiring substrate has the wirings formed on the main surface of a substrate base material (tape), and an elastic structural material is disposed opposite to the main surface of the substrate base material.

Further, the bump electrodes are formed on the side of the wirings.

Further, the bump electrodes are connected with the wirings each by way of a through hole disposed in an insulation film formed on the wirings and having a thickness smaller than that of the wiring base material.

Further, the external terminals of the semiconductor chip are disposed to a central portion or an outer circumferential portion of the semiconductor chip, and the bump electrodes connected to the external terminals of the semiconductor chip by way of the wirings of the wiring substrate are disposed to the inside, outside or both regions of the inside and the outside to the outer circumference of the semiconductor chip.

Further, in a semiconductor integrated circuit device of the present invention, the size for the end of the elastic structural member of the semiconductor chip on the side of

the externals terminal and the end of the substrate base material of the wiring substrate is determined based on the ingredients of the elastic structural material.

Further, in a semiconductor integrated circuit device of the present invention, a distance M2 between the end of the substrate base material of the wiring substrate and the end of the elastic structural material on the outer circumferential side of the semiconductor integrated circuit device, and a distance M1 between the end of the semiconductor chip and the end of the substrate base material are determined within a range capable of satisfying the relationship:

$$M1 > M2 > 0$$

Further, in a semiconductor integrated circuit device of the present invention, the wirings of the wiring substrate are formed to such a shape that a portion fixed with the substrate base material of the wiring substrate and a top end portion connected to the external terminals of the semiconductor chip are displaced at least by more than the width of the wirings.

Further, in a semiconductor integrated circuit device of the present invention, the wirings of the wiring substrate is formed as a cantilever structure fixed at one side to the substrate base material of the wiring substrate.

Further, in a semiconductor-integrated circuit device of the present invention, the size for the end of an opening

in a surface protection film on the semiconductor chip is determined within such a range that the wirings do not interfere the surface protection film at least on the side of driving down a bonding tool when the bonding tool is driven down.

Further, in a semiconductor integrated circuit device of the present invention, the wirings of the wiring substrate is formed such that an effective area of a wiring portion of the wiring on the side of the notch terminal end is made greater. Particularly, the wiring portion on the side of the notch terminal end is connected with an opposed land portion of the wirings, or extended longitudinally or laterally in a vacant region of the wirings, or adjacent wirings are connected with each other.

Further, in a semiconductor integrated circuit device of the present invention, the elastic structural material is formed within a range greater over the entire circumference at least by more than the with of the protrusion at the outer circumferential portion formed to the elastic structural material.

Further, in a semiconductor integrated circuit device of the present invention, when the elastic structural material is formed by dividing so as not to be bonded on the external terminals of the semiconductor chip, each of the ends of spaces to which the divided elastic structural materials

are opposed is formed in a groove-shape. Particularly, a plurality of grooves are formed to each of the ends of the elastic structural material, or a stepping dam for sealant flow is previously formed upon sealing step.

Further, in a semiconductor integrated circuit device of the present invention, the connection structure between the external terminals of the semiconductor chip and the wirings of the wiring substrate are formed by previously forming a stud bumps to the external terminal of the semiconductor chip, and the external terminals of the semiconductor chip and the wirings of the wiring substrate are connected by way of the stud bumps.

Further, in a semiconductor integrated circuit device of the present invention, the connection structure between the external terminals of the semiconductor chip and the wiring substrate is formed by previously supplying solder so as to surround the wirings of the wiring substrate and the external terminals of the semiconductor chip and the external terminals of the semiconductor chip are connected by way of the solder.

Further, in a semiconductor integrated circuit device of the present invention, the connection structure between the external terminal of the semiconductor chip and the wirings of the semiconductor substrate are formed by connecting the wirings of the wiring substrate and the external

terminals of the semiconductor chip by way of the stud bumps by using stud bumps of solder or Au ball so as to surround the wirings of the wiring substrate from above.

Further, in a semiconductor integrated circuit device of the present invention, the connection structure between the external terminals of the semiconductor chip and the wirings of the wiring substrate are formed by connecting the wirings of the wiring substrate and the external terminals of the semiconductor chip by using Al, solder or Au wire.

Further, in a semiconductor integrated circuit device of the present invention, the wiring structure of the wiring substrate is formed narrowing the lateral size of the wirings from the end of the substrate base material of the wiring substrate to the top end of the wirings, such that the bending stress ratio α is represented by:

$$\alpha = \sigma 1/\sigma 0$$

where $\sigma 0$ is bending strength caused at the end of the substrate base material and $\sigma 1$ is maximum stress caused to an intermediate portion between the end of the substrate base material and the top end of the wirings, and such that the lateral size is made constant particularly from a predetermined position, and the size and the shape of the wirings are determined such that the bending stress ratio α is from 1.2 to 1.5 in a case where the bending stress ratio α is represented by the following formula:

$$\alpha = b1 \times (L2 - L1)/(b2 \times L2)$$

in which L1 is a taper length, L2 is a wiring length, b1 is a taper width and b2 is a wiring width.

Further, in a semiconductor integrated circuit device of the present invention, the wiring structure of the wiring substrate is formed by using an electroconductive material as a core material and applying Au plating on the surface.

Further, the wiring structure of the wiring substrate is formed by using Cu as a core material, applying Au plating on the surface and making at least one end connected with the external electrodes of the chip into a S-shaped configuration.

Further, in a semiconductor integrated circuit device of the present invention, a flattening insulation film is formed to the wiring substrate on the side of the wirings and an elastic structural material is disposed on the insulation film.

Further, a method of manufacturing a semiconductor integrated circuit device according to the present invention comprises a step of forming an elastic structural material on the rear face of a wiring substrate (tape side) in which wirings are formed on the substrate base material (tape), a step of bonding a semiconductor chip to the surface of the elastic structural material so as to oppose to the wiring substrate, a step of connecting one end of the wirings to the external terminals of the semiconductor chip, a step of

forming an insulation film thinner than the substrate base material on a main surface of the wirings, a step of forming openings to the insulation film each at a position corresponding to the other end of the wirings to be joined with the bump electrodes, and a step of forming the bump electrodes being joined to the other end of the wirings by way of the wirings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view illustrating a semiconductor integrated circuit device as an Embodiment 1 of the present invention;

Fig. 2 is a cross sectional view taken along line A-A' in Fig. 1 of the Embodiment 1 according to the present invention;

Fig. 3 is a plan view illustrating the state of mounting the semiconductor integrated circuit device in the Embodiment 1 according to the present invention to a mounting substrate;

Fig. 4 is a cross sectional view illustrating the state of mounting the semiconductor integrated circuit device in the Embodiment 1 according to the present invention to a mounting substrate;

Fig. 5 is a flow chart illustrating a step of assembling the semiconductor integrated circuit device in the Embodiment

1 according to the present invention;

Fig. 6 is a cross sectional view for a main portion of the semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 7 is a cross sectional view for a main portion for comparative explanation of the semiconductor integrated circuit device of the Embodiment 1 according to the present invention and a semiconductor integrated circuit device studied by the present inventor;

Fig. 8 is a cross sectional view for a main portion illustrating both face wirings as a modified embodiment of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 9 is a plan view illustrating a window opening portion of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 10 is a cross sectional view corresponding to the window opening in Fig. 9;

Fig. 11 is a cross sectional view for explaining the size of a window opening and an edge portion of the semiconductor chip in a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 12 is a cross sectional view illustrating a concave of an elastomer after printing of a semiconductor integrated

circuit device in the Embodiment 1 according to the present invention;

Fig. 13 is a cross sectional view illustrating a tape warping after appending a semiconductor chip in a semiconductor integrated circuit device of the Embodiment 1 according to the present invention;

Fig. 14 is a plan view illustrating a planer S-shaped lead of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 15 is a cross sectional view taken along arrow B in Fig. 14 of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 16 is a cross sectional view taken along arrow A in Fig. 14 in a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 17 is a cross sectional view illustrating a trace of a bonding tool upon forming a standard S-shaped lead in a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 18 is a cross sectional view illustrating a trace of a bonding tool upon forming a planer S-shaped lead in a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 19 is a plan view for explaining a notch lead and a beam lead of a semiconductor integrated circuit device in

the Embodiment 1 according to the present invention;

Fig. 20 is a plan view illustrating a notch lead at the portion A in Fig. 19 of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 21 is a plan view illustrating a beam lead of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 22 is a cross sectional view illustrating a lead bonding portion of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 23 is a plan view illustrating a lead bonding portion of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 24 is a cross sectional view illustrating, in an enlarged scale, a landing position of a tool in the portion A in Fig. 22, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 25 is a cross sectional view illustrating a bonding portion improved for the size of a passivation opening, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 26 is a plan view illustrating a bonding portion for a bothway lead, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 27 is a plan view illustrating standard anchor

wirings, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 28 is a plan view illustrating improved anchor wirings, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 29 is a perspective view illustrating a structure of a standard elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 30 is a perspective view illustrating a state of appending a semiconductor chip at a standard elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 31 is a perspective view illustrating a structure of a wide elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 32 is a perspective view illustrating a state of appending a semiconductor chip at a wide elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 33 is a cross sectional view illustrating a state of appending a semiconductor chip at a wide elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 34 is a perspective view illustrating a structure

of the standard elastomer after appending a semiconductor chip, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 35 is a cross sectional view illustrating a structure of a standard elastomer after appending the semiconductor chip, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 36 is a perspective view illustrating a structure of a wide elastomer after appending the semiconductor chip, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 37 is a cross sectional view illustrating a structure of a wide elastomer after appending the semiconductor chip, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 38 is a cross sectional view illustrating a concept of metal mask printing, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 39 is a plan view illustrating a metal mask of a standard elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 40 is a plan view illustrating a metal mask of a wide elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 41 is a plan view illustrating a printed shape for a plurality of suspended wide elastomers, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 42 is a plan view illustrating a potting position for groove-fillage of a wide elastomer, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 43 is a cross sectional view illustrating a bonding portion by a standard lead bonding, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 44 is a cross sectional view illustrating a bonding portion by using stud bumps, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 45 is a cross sectional view illustrating a lead connection by using solder, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 46 is a plan view illustrating a lead connection using solder, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 47 is a cross sectional view illustrating a lead connection by using solder or Au ball, of a semiconductor

integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 48 is a perspective view illustrating a lead connection by using solder or Au ball, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 49 is a cross sectional view illustrating a lead connection by using Al or soldering wire, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 50 is a cross sectional view illustrating a lead connection by using an Au wire, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 51 is a perspective view explaining a lead design, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 52 is a perspective view illustrating modification of lead after bonding, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 53 is an explanatory view illustrating a relationship between a lead size and a bending stress ratio, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 54 is a cross sectional view illustrating a

connection portion of lead connection, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 55 is an enlarged cross sectional view illustrating a lead bent portion, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 56 is an enlarged cross sectional view illustrating a Ni-platingless lead bent portion, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 57 is an enlarged cross sectional view illustrating a lead press contact portion, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 58 is an enlarged cross sectional view illustrating a Ni-platingless lead press contact portion, of a semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 59 is a cross sectional view illustrating a structure of a semiconductor integrated circuit device in an Embodiment 2 according to the present invention;

Fig. 60 is a perspective view illustrating a structure of a semiconductor integrated circuit device in the Embodiment 2 according to the present invention;

Fig. 61 is a plan view, as viewed from the rear face of

a semiconductor chip, of a semiconductor integrated circuit device in the Embodiment 3 according to the present invention;

Fig. 62 is a plan view illustrating a semiconductor integrated circuit device in the Embodiment 3 according to the present invention;

Fig. 63 is a cross sectional view illustrating a semiconductor integrated circuit device in the Embodiment 3 according to the present invention;

Fig. 64 is an enlarged cross sectional view illustrating a portion A in Fig. 63, of a semiconductor integrated circuit device in the Embodiment 3 according to the present invention;

Fig. 65 is a plan view for explaining a wiring structure of a wiring substrate, of a semiconductor integrated circuit device in the Embodiment 3 according to the present invention;

Fig. 66 is a plan view, as viewed from the rear face of a semiconductor chip, of a semiconductor integrated circuit device as an Embodiment 4 according to the present invention;

Fig. 67 is a plan view illustrating a semiconductor integrated circuit device in the Embodiment 4 according to the present invention;

Fig. 68 is a cross sectional view illustrating a semiconductor integrated circuit device in the Embodiment 4 according to the present invention;

Fig. 69 is an enlarged cross sectional view illustrating a portion A in Fig. 68, of a semiconductor integrated

circuit device in the Embodiment 4 according to the present invention;

Fig. 70 is a plan view for explaining a wiring structure of a wiring substrate, of a semiconductor integrated circuit device in the Embodiment 4 according to the present invention

Fig. 71 is a plan view, as viewed from the rear face of a semiconductor chip, of a semiconductor integrated circuit device in the Embodiment 5 according to the present invention;

Fig. 72 is a plan view illustrating a semiconductor integrated circuit device in the Embodiment 5 according to the present invention;

Fig. 73 is a cross sectional view illustrating a semiconductor integrated circuit device in the Embodiment 5 according to the present invention;

Fig. 74 is an enlarged cross sectional view illustrating a portion A in Fig. 73, of a semiconductor integrated circuit device in the Embodiment 5 according to the present invention;

Fig. 75 is a plan view for explaining a wiring structure of a wiring substrate, of a semiconductor integrated circuit device in the Embodiment 5 according to the present invention;

Fig. 76 is a cross sectional view illustrating the modified shape of the lead in accordance with the bending stress ratio in a comparative explanation between the semiconductor integrated circuit device in the Embodiment 1 according to the present invention and the semiconductor

circuit device studied by the present inventors;

Fig. 77 is a cross sectional view illustrating the modified shape of the lead in accordance with the bending stress ratio, of the semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 78 is a cross sectional view illustrating the modified shape of the lead in accordance with the bending stress ratio, of the semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 79 is a cross sectional view illustrating the modified shape of the lead in accordance with the bending stress ratio, of the semiconductor integrated circuit device in the Embodiment 1 according to the present invention;

Fig. 80 is a cross sectional view illustrating the modified shape of the lead in accordance with the bending stress ratio, of the semiconductor integrated circuit device in the Embodiment 1 according to the present invention; and

Fig. 81 is a cross sectional view illustrating a modified example of a package structure, of the semiconductor integrated circuit device in the Embodiment 1 according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described more specifically by way of preferred embodiments with reference

to the drawings.

Embodiment 1

Fig. 1 is a plan view illustrating a semiconductor integrated circuit device as an Embodiment 1 according to the present invention, Fig. 2 is a cross sectional view taken along line A-A' in Fig. 1, Fig. 3 and Fig. 4 are plan view and a cross sectional view illustrating a state of mounting a semiconductor integrated circuit device to a mounting substrate, Fig. 5 is a flow chart illustrating a step of assembling a semiconductor integrated circuit device, Fig. 6 to Fig. 58, Fig. 76 to Fig. 81 are views for comparative explanation between the feature of the semiconductor integrated circuit device in the Embodiment 1 of the present invention and a semiconductor integrated circuit device as a comparative example studied by the present inventor. Explanation for the views are made on every technical items to be described later.

At first, explanation will be made to the constitution of a semiconductor integrated circuit device of an Embodiment 1 with reference to Fig. 1 to Fig. 2.

The semiconductor integrated circuit device as the Embodiment 1 of the present invention is in the form of a 40 pin ball grid array type semiconductor package, comprising a semiconductor chip 1 having a plurality of semiconductor

elements and a plurality of bonding pads formed on a main surface, and an elastomer 2 (elastic structural material) bonded on the main surface of the semiconductor chip excepting for the portions of forming the bonding pads, a flexible wiring substrate 3 (wiring substrate) formed with wirings connected at one end to the bonding pads of the semiconductor chip 1, a solder resist 4 (insulation film) formed on a main surface of the flexible wiring substrate 3, and bumps 5 (bump electrodes) formed on a main surface of the solder resist 4 and connected the other end of the wirings by way of openings in the solder resist 4, to constitute a package structure in which the bonding portion of the semiconductor chip 1 is covered by a sealant 6 such as a resin.

The semiconductor chip 1 has, for example, a center pad structure as shown in Fig. 1 in which a plurality of bonding pads 7 (external terminals) are formed in one row to a central portion in the longitudinal direction, and the bonding pads are arranged each at a not-uniform interval. Predetermined integrated circuits such as memory circuits and logic circuits are formed to the semiconductor chip 1, for example, on a semiconductor substrate such as made of silicon and the bonding pads 7 made of a material such as Al are disposed as the external terminals for such circuits.

The elastomer 2 is made of an elastic material, for example, a silicone resin, which is formed on the main

surface of the semiconductor chip 1 being bisected into both longitudinal ends of the chip 1 excepting for the portion formed with the bonding pads 7 and bonded to the main surface of the chip 1 by way of adhesives 8. The elastomer 2 is provided for moderating stress concentration to the soldering bumps 5 mainly caused by the difference of heat expansion coefficients of the semiconductor chip 1 and the package mounting substrate.

The flexible wiring substrate 3 comprises, for example, as shown in Fig. 2, a tape 9 as a basic material of the flexible wiring substrate 3 (substrate base material) and wirings 10 bonded on the main surface of the tape 9 by adhesives 9', in which leads 11 on one end of the wirings 10 are connected to the bonding pads 7 of the semiconductor chip 1, and bump lands 12 on the other end are connected with the soldering bumps 5. In the flexible wiring substrate 3, the rear face of the tape 9 (on the side opposite to the surface formed with the wirings 10) is bonded to the elastomer 2, and the solder resist 4 is formed to the main surface of the wirings 10.

The tape 9 constituting the flexible wiring substrate 3 is made of a material, for example, a polyimide resin, and a material such as Cu is used as the core material for the wiring 10. A portion of the lead 11 as one end of the wiring 10 is formed with an Ni plating layer so as to cover

the surface of the core material, and an Au plating layer is formed further so as to cover the surface of the Ni plating layer.

The solder resist 4 is made of an insulation material such as a light sensitive epoxy resin, and the solder bumps 5 are formed on the main surface of the wirings 10 of the flexible wiring substrate 3 by way of the openings in the solder resist 4 for a predetermined range of the wirings 10 excepting for the connection portion connected to the bump lands.

The soldering bumps 5 are made of a material, for example, a Pb(560%) - Sn(40%) solder or an alloyed solder mainly composed of Pb - Sn, and connected to the bump lands 12 of the wirings 10 constituting the flexible wiring substrate 3. The solder bumps 5 are disposed being arranged each by two rows in the regions on both side of the bonding pads 7 of the semiconductor chip 1.

The thus constituted semiconductor integrated circuit device is mounted, for example, as shown in Fig. 3 and Fig. 4, as a semiconductor integrated circuit device of a chip size package 13, for example, DRAM, together with a semiconductor integrated circuit device of QFP type package 14 to a mounting substrate 15 which is made, for example, of glass or epoxy on a memory card and can be retractably mounted to a portable equipment such as a portable telephone

or a handy type personal computer by way of external connection terminals 16.

For the function of the Embodiment 1 of the present invention, the outline for the steps of assembling the semiconductor package will be explained on the basis of the process flow shown in Fig. 5.

At first, before assembling the semiconductor package, wirings 10 are formed on the tape 9, the flexible wiring substrates having the leads 11 formed by etchings portion of the wirings 10, the elastomer 2, the semiconductor chip 1 formed with a predetermined integrated circuits and provided with the bonding pads 7 as external terminals, the sealant 6 flux and solder forming the solder balls 17 are provided.

The flexible wiring substrate 3 can be prepared, for example, as typically represented by the technique of a TAB (Tape Automatic Bonding) tape, by bonding a thin metal foil such as made of Cu on the tape 9 made of a polyimide resin by means of an adhesive, forming a required pattern by photoresist on the metal foil using photographic technique, then forming a requiring wiring pattern 10 by etching (including also leads 11) and, further, applying Ni-Au plating treatment to the surface thereof, for example, by an electric field plating method.

Then, for example, the elastomer 2 is formed by printing to a thickness of 50 to 150 μm on the tape 9 of the flexible

wiring substrate 3, and a silicone type adhesives 8 are coated and printed on the surface of the elastomer 2 (steps 501, 502). The elastomer 2 is not always printed but an elastomer previously formed into a film-shape may be cut into a predetermined shape and bonded to the rear face of the tape 9 by means of the adhesives 8.

Further, the leads 11 at one end of the wirings 10 of the flexible wiring substrate 3 and the bonding pads 7 of the semiconductor chip 1 are aligned such that their relative positions coincide with each other, and the semiconductor chip 1 is appended by adhesion to the elastomer 2 printed on the tape 19 of the flexible wiring substrate 3 (step 503).

Then, they are turned upside down in a state where the semiconductor chip 1 and the tape 9 of the wiring substrate 3 are appended by way of the elastomer 2, the semiconductor chip 1 and the tape 9 of the flexible wiring substrate 3 in a state appended by way of the elastomer 2 are turned upside down in the lead bonding step, the lead 11 is driven down on the bonding pad 7 of the semiconductor chip 1 while being deformed into a S-shaped configuration by a bonding tool 18 as shown by the cross section in Fig. 2, and the lead 11 and the bonding pad 7 are connected, for example, by a method of supersonic thermal press bonding (step 504)

Successively, in the sealing step, the lead bonding portion of the bonding pad 7 of the semiconductor chip 1 and

the lead 11 of the flexible wiring substrate 3 are resin encapsulated, for example, by coating the sealant 6 such as made of an epoxy resin from a dispenser 19 to thereby enhance the reliability at the junction portion between the semiconductor chip 1 and the flexible wiring substrate 3 (step 505).

Subsequently, in the cutting step for the flexible wiring substrate 3, the outer edge portion of the tape 9 is cut along a position somewhat outer to the edge of the semiconductor chip 1, to form a package outer shape of CSP (Chip Size Package or Chip Scale Package) (step 506).

Then, in the bump attaching step of the solder bump 5, the bump 5 is formed by joining a solder ball 17 to the corresponding bump land 12 of the wirings 10 of the flexible wiring substrate 3 to form the bump 5 and, finally, by way of the selection and marking, the step of assembling the semiconductor package in the Embodiment 1 according to the present invention is finished (step 507, 508).

In the step of assembling the semiconductor package, the order of the tape cutting step (step 506) and the bump attaching step (step 507) may be reversed.

Thus, the Embodiment 1 has a semiconductor package structure in which bonding pads 7 are arranged concentrically in one row to a central portion of the semiconductor chip 1, and the solder bumps 5 are disposed at the inside of the outer circumference of the semiconductor chip 1 connected by

way of the wirings 10 of the flexible wiring substrate from the bonding pads 7.

Then, the feature of the package structure for the semiconductor integrated circuit device of the Embodiment 1 will be explained by comparison with the package structure as the technique studied by the present inventor including the structure and the process with reference to Fig. 6 to Fig. 58 successively.

1. Surface Wiring Structure (a structure in which the elastomer is formed to the wiring substrate on the side of the tape and the bump electrodes are formed on the side of the wirings).

In the technical explanation for the surface wiring structure, Fig. 6 is a cross sectional view for a main portion illustrating the surface wiring structure, Fig. 7 is a cross sectional view for a main portion illustrating the rear face wiring structure (a structure in which bump electrodes are formed to the wiring substrate on the side of the tape and the elastomer is formed on the side of the wirings) and Fig. 8 is a cross sectional view for a main portion illustrating wirings on both surfaces.

The package structure of the Embodiment 1 is a so-called surface wiring structure as shown in an enlarged scale in Fig. 6, in which an elastomer 2 is bonded to a

flexible wiring substrate 3 on the side of a tape 9 (on the side of a semiconductor chip 1) and a solder resist 4 and a bump electrode 5 are formed on the side of wirings 10. On the contrary, the technique studied by the present inventor is a so-called rear face wiring structure, as shown in Fig. 7, in which an elastomer 2 is bonded on the side of wiring 10 and a solder bump 5 is formed on the side of a tape 9. In Fig. 6, an Au plating 11a is formed, for example, by an electric field plating to the surface of a lead 11 on one end and on the surface of a land 12 on the other end of the wiring 10.

In the rear face wiring structure described above, a through hole 12b for joining the bump 5 is formed, for example, by punching out the tape 9 made of a material such as a polyimide resin, whereas in the surface wiring structure of the Embodiment 1, a solder resist 4 made of a material such as a light sensitive epoxy resin is coated on the main surface of the wiring 10, and a connection hole 12a of a desired size is formed at a desired position by a photographic process such as exposure and development, so that the following advantages can be expected.

(1) Since the opening for the solder bump 5 is formed by exposure and development of the solder resist 4, the fabrication accuracy for the hole diameter can be improved compared with a case of puncturing the opening to the tape 9 of

the flexible wiring substrate 3 in the rear face wiring structure by machining.

(2) While the practically minimum thickness of the tape 9 is about 50 μm, the solder resist 4 can be coated to a thickness of about 10 to 20 μm stably depending on the coating condition, so that a smaller solder ball 17 can be joined satisfactorily.

For example, in a case of forming a solder bump of about 30 μm diameter which is less than the thickness of the tape 9, the aspect ratio of the through hole is excessively large in the rear face wiring structure to possibly cause connection failure. On the other hand, the aspect ratio can be lowered to cope with such a problem in the surface wiring structure.

(3) Since the arrangement pitch of the solder bumps 5 can be made smaller in the surface wiring structure as compared with the rear face wiring structure, a semiconductor package having output terminals for the solder bumps at a higher density can be constituted.

(4) Since the elastomer 2 is disposed to the flat surface at the back of the tape 9, the elastomer 2 can be mounted (coated or appended) in a voidless manner stably at a high accuracy. Further, since the size and the shape of the elastomer 2 are stabilized, the bonding step of the semiconductor chip 1 is also stable, thereby enabling to

conduct assembling at higher yield.

As described above, the technique of the rear face wiring structure results in problems such as in the formation of the opening to the tape 9 of the flexible wiring substrate 3 and bondability between the wirings 10 of the flexible wiring substrate 3 and the elastomer 2, whereas such problems can be solved by adopting the surface wiring structure in the Embodiment 1.

Further, in the wiring structure of the flexible wiring substrate 3, it is possible to use a flexible wiring substrate 3 having a both face wiring structure, for example, as shown in Fig. 8, that is, having two layered wirings on both surfaces of the tape 9, in addition to the single face wiring structure as shown in Fig. 6, and it can be applied further widely to three or more layered wiring structures.

In the example of Fig. 8, a first wiring 20 is used as a signal wiring while the second wiring 21 is used as a ground plane, in which the second wiring 21 and the bump 5 or the first wiring 20 are electrically connected by way of a via hole 22. Such a structure has a merit capable of obtaining excellent electric characteristic, for example, in view of the noise resistance.

2. Optimization of tape eave to elastomer

In the technical explanation for optimization of tape

eave to the elastomer, Fig. 9 is a plane view illustrating window openings, Fig. 10 is a cross sectional view illustrating a window opening in Fig. 9 and Fig. 11 is a cross sectional view for the explanation of the size for the window opening portion and the edge portion of the semiconductor chip.

The package structure of the Embodiment 1, as shown in Fig. 9, has a BGA (Ball Grid Array) structure in which the solder bumps 5 are arranged in a matrix on the main surface of the flexible wiring substrate 3. In this example, as shown in Fig. 10, the semiconductor 1 has a center pad arrangement in which an window opening portion 23 is disposed longitudinally at a central portion, and the portion and the peripheral edge of the semiconductor chip 1 are resin capsulated by the sealant 6 to attain a structure of high moisture proofness and reliability in the final structure.

By the way, in the technique studied by the present inventor, when the end of the elastomer 2 (on the side of the window opening 23 is brought closer to the edge of the tape 9, that is, if the size L1 between the end of the elastomer 2 of the semiconductor chip 1 on the side of the bonding pad 7 and the end of the tape 9 is reduced, contamination to the lead 11 due to the bleeding ingredient and the volatile ingredient of the elastomer 2 is caused.

On the other hand, if the size L1 is made larger, that is, if the elastomer is excessively retracted from the edge of the tape 9, the size L2 between the end of the elastomer 2 and the solder bump 5 is reduced and since the elastomer 2 is not present below the innermost solder bump 5, this may possibly worsens the variation in the height of the solder bump 5 or widen the encapsulation region for the window opening 23 making it difficult to fill the sealant 6.

On the contrary, in the Embodiment 1, the problems can be solved simultaneously by selecting the appropriate size for L1 and disposing the end of the elastomer 2 at an optimal position between the end of the tape 9 and the solder bump 5.

That is, since the foregoing problems are present for the window opening 23, the size is defined as below. For example, in this embodiment, the printing accuracy of the elastomer 2 is defined as about $\pm$100 μm. Accordingly, if the size L1 is less than 100 μm, since it is out of the tape 9 by printing deviation, it must be greater than the printing accuracy (100 μm) at the least.

Further, since there is no problem for the contamination to the lead 11 by the bleeding ingredient or volatile ingredient of the elastomer 2 if it is actually spaced apart by about 300 μm from the actual result, it is determined, for example, as 300 μm at the minimum. However, a design with the minimum value of about 100 μm is possible if the elastomer

2 of less contamination and bleeding is used or a counter-measure, for example, cleaning of contamination is taken.

As described above, contamination to the lead 11 caused by the bleeding ingredients or volatile ingredients of the elastomer 2 can be prevented, the variation in the height of the solder bumps 5 can be made stable and the sealing region of the window opening 23 can be filled with ease by selecting an appropriate size L1 as the Embodiment 1.

3. Optimization for the outer size of package

In the technical explanation for the optimization of the outer size of the package, Fig. 11 is a cross sectional view for explaining the size of the window opening and the edge portion of the semiconductor chip, Fig. 12 is a cross sectional view illustrating a concave of the elastomer after printing and Fig. 13 is a cross sectional view illustrating a warp of a tape after appending a semiconductor chip.

For example, in the technique studied by the present inventor, in Fig. 11, assuming a the distance between the end of the semiconductor chip 1 on the outer circumference of the package and the end of the tape 9 of the flexible wiring substrate 3 as M1 and a distance between the end of the elastomer 2 and the end of the tape 9 as M2, the following problems are present:

(1) If M1 < 0, since the outermost circumference of the

package is that of the semiconductor chip 1, there is a great possibility of inducing cracks to the semiconductor chip 1 in the assembling step, upon insertion and withdrawal of a receptacle, during tray transportation and the like.

(2) If M1 < 0, M2 > 0, since the circuit surface of the semiconductor chip 1 is exposed to the outside, a problem is caused to the reliability and the sealing for preventing this, although possible leads to increase of the steps.

(3) If M1 - Me < 0, peripheral protrusions of the elastomer 2 after printing shown in Fig. 12 interferes the bonding portion of the semiconductor chip 1 as shown in Fig. 13 to cause bonding failure upon appending, worsening of flatness for the flexible wiring substrate 3 and reduction of the reliability.

(4) If M2 = 0, it is necessary to cut the elastomer 2 to cause a problem in the difficulty of cutting.

On the contrary, in the Embodiment 1, the foregoing problems can be overcome by determining the relationship for the distance between the end of the semiconductor chip 1 or the end of the elastomer 2 and end of the tape 9 as: M1 > M2 > 0 That is, in the explanatory view for the size illustrating the edge portion of the package in Fig. 11, since the cutting error in the tape cutting step for determining the final outer shape is about 100 μm, it is desired to ensure more than 100 μm for M2 in order that the cutting jig does not

reach the elastomer 2.

By the way, the cross sectional shape after forming the elastomer 2 by printing and hardening the same by baking is as shown in Fig. 12, and a peripheral portion tends to be higher being pulled by a mask upon leaving a plate after printing in a case of a material having a thixotropic property which is higher to some extent. For example, if the semiconductor chip 1 is appended under the condition as M1 < M2 in which the end of the semiconductor chip is smaller than the end of the elastomer 2, a problem that the surface of the tape 9 warps conforming the cross sectional shape of the elastomer 2 is caused as shown in Fig. 13.

In order to prevent this, it is effective to escape a high peripheral portion of the elastomer 2 to the outside of the semiconductor chip 1 by determining as: M1 > M2. For instance, since the width of the protrusion is about 200 μm, it is desired that (M1 - M2) is 240 μm, and the distance M1 is about 360 μm in view of the distance M2 = 100 μm for the cutting property.

Cutting the tape 9 at the outer circumference as described above provides advantages that the outer shape error is reduced, and peripheral jigs such as a receptacle or a tray may not be changed for the change of the size to some extent of the semiconductor chip 1.

As described above, in the Embodiment 1, it is possible

to avoid cracking and chipping of the semiconductor chip 1 to improve the cutting margin in the cutting step. Further, the circuit surface of the semiconductor chip 1 can be entirely disposed below the elastomer 2 to provide a merit of improving the moisture proofness and eliminating the requirement for sealing to the outer circumferential portion.

4. Planer S-shaped lead

In the technical explanation for the planer S-shaped lead, Fig. 14 is a plan view illustrating a planer S-shaped lead, Fig. 15 is a cross sectional view taken along arrow B in Fig. 14, Fig. 16 is a cross sectional view taken along arrow A in Fig. 14, Fig. 17 is a cross sectional view illustrating a trace of a bonding tool upon forming a standard S-shaped lead and Fig. 18 is a cross sectional view illustrating a trace of a bonding tool upon forming a planer S-shaped lead.

The S-shaped configuration is such a structure in which the length of a lead 11 at one end of a wiring 10 is substantially made longer than a linear distance between a pad 7 of a chip 1 and an edge portion 11b of a tape 9, so that stresses on the lead 11 can be reduced.

For example, in the technique of forming a standard S-shaped lead 24 studied by the present inventor, the lead is a linear notch lead or a beam lead as shown by the dotted

line in Fig. 14, and in order to form a sag (S-shaped configuration) enough to withstand thermal deformation as shown by a fine line in Fig. 15 after bonding, it is necessary for such a motion as along a special bonding tool trace 25 of once driving down the lead 11 just above the semiconductor chip 1, laterally displacing and then again driving down it onto the bonding pad 7 which may require an exclusive wire bonder.

On the contrary, in the Embodiment 1, the foregoing problem can be solved by preparing the lead 11 of the wiring 10 not a linear shape but as a planer S-shaped lead 26 of a S-shaped configuration in which the base portion of the wiring 10 and the bonding portion at the top end are previously displaced at least by more than the width of the lead 11 as shown in Fig. 14, upon forming the wiring 10 on the tape 9 of the flexible wiring substrate 3.

As described above by forming the planer S-shaped lead 26, a planer S-shaped lead 26 of a stable and suitable S-shaped configuration can be formed by a bonding tool trace 25 by simply driving down a usual wire bonder as shown in Fig. 18, since a sag due to the original planer S-shaped configuration is formed as shown in Fig. 16, although a straightened shape as shown in Fig. 15 is formed.

This can form the planer S-shaped lead 26 of the stable S-shaped configuration with no requirement for a soft-

modified special wire bonder and, further, an effect for shortening the tact time upon bonding can also be expected since the bonding tool trace 25 can also be simplified.

5. Beam lead

In the technical explanation for the beam lead, Fig. 19 is a plan view for explaining a notch lead and a beam lead, Fig. 20 is a plan view illustrating a notch lead in a portion A of Fig. 19 and Fig. 21 is a plan view illustrating a beam lead.

For example, in the technique studied by the present inventor, as shown in Fig. 20 which is an enlarged view for the lead 11 in Fig. 19, a lead 11 is formed with a notch 27, for example, of a V-shaped cut at a cutting portion. A portion slightly inside of the notch 27 is driven downwardly by a bonding tool 18 upon bonding, to cut the lead 11 at the portion of the notch 27. However, the width of the notch 27 changes due to varied etching for the wiring 10 in the manufacturing step for the flexible wiring substrate 3 failing to cut upon bonding.

Further, even if it can be cut, it may be considered to cause such a problem that the lead is cut at a portion different from the desired notch 27, or the notch is too narrow and disconnected before the plating step of the flexible wiring substrate 3 and can not be plated.

On the contrary, in the Embodiment 1 as shown in Fig. 21, the problem upon cutting the lead 11 as described above can be overcome by making the lead as a cantilever beam structure, namely, a so-called beam lead 28 in which one end is fixed to the tape 9 of the flexible wiring substrate 3 and the end as the cutting side formed with the notch 27 is left open.

6. Passivation size for the periphery of bonding pad

In the technical explanation for the size of the passivation film at the periphery of the bonding pad, Fig. 22 is a cross sectional view illustrating a lead bonding portion, Fig. 23 is a plan view illustrating a lead bonding portion, Fig. 24 is a cross sectional view illustrating a tool landing point at the portion in Fig. 22 in an enlarged scale, Fig. 25 is a cross sectional view illustrating a bonding portion improved for the size of the passivation opening and Fig. 26 is a plan view illustrating a bonding portion of a both way lead.

In a memory chip typically represented by DRAM or the like, a passivation film 29 made of a polyimide type resin is formed on the chip for preventing soft errors caused by α-rays.

For example, in the technique studied by the present inventor, since the lead 11 is once driven downwardly just

above the semiconductor chip 1, then displaced laterally and again driven downwardly on the bonding pad 7 of the semiconductor chip 1 as shown by the bonding tool trace 25 in the bonding sequence as shown in Fig. 22, Fig. 23 and Fig. 24, it may be considered to such a problem that the passivation 29 on the semiconductor chip 1 or the semiconductor chip 1 therebelow undergoes damages by the first driving down, or ingredients of the passivation 29 are deposited to contaminate the bonding portion on the lower surface of the lead 11 to worsen the bondability.

On the contrary, in the Embodiment 1, the foregoing problems can be solved by extending the distance L3 from the opening edge of the bonding pad 7 to the edge of the passivation film 29 on the side of the bonding pad 7 shown in Fig. 22, Fig. 23, Fig. 24 such that the passivation opening 30 is enlarged and the lead 11 does not interfere with the passivation film 29 at least on the side of driving down the bonding tool 18 to make an improvement as shown in Fig. 25.

That is, in Fig. 24, the size L3 is about 25 μm in an example of a semiconductor chip 1, for example, a memory. For instance, since the size of the bonding pad 7 is 100 μm square and the size of the top end of the bonding tool 18 is equal with or less than that, a retraction amount L3 of the passivation 29 in Fig. 25 is desirably, for example, about more than 125 μm.

As described above, a suitable bonding property can be attained without giving damages to the passivation 29 on the semiconductor chip 1 or the semiconductor chip 1 or without deposition of ingredients of the passivation 29 to the bonding portion at the lower surface of the lead 11 to cause contamination.

Further, also in a case where the leads 11 extend from both directions, the problem can also be coped similarly by enlarging the distance from the opening edge of the bonding pad 7 to the edge of the passivation 29 on the side of the bonding pad 7 at least on the side of driving down the bonding tool. Enlargement between the edges caused no problem even if applied to the opposite side to such an extent as not exposing the circuit surface of the semiconductor chip 1.

7. Improvement of anchor wiring

In the technical explanation for the improvement of the anchor wiring, Fig. 27 is a plan view illustrating a standard anchor wiring and Fig. 28 is a plan view illustrating an improved anchor wiring.

For example, in the technique studied by the present inventors, in a pattern of a standard anchor wiring 31 on the terminal end of a notch as shown in Fig. 27, if the notch 27 is formed greater than a designed value, such a

disadvantage may be considered that the lead is not cut at the portion of the notch 27 but the bonding strength between the wiring 10 and the tape 9 ahead of the notch in the standard anchor wiring 31 is yielded and the portion of the standard anchor wiring 31 is peeled from the tape 9.

On the contrary, in this Embodiment 1, the bonding strength between the wiring 10 and the tape 9 can be increased to obtain a stable cutting performance of the notch 27 by providing an enlarged anchor wiring 32 for enlarging the effective area in the portion for the anchor wiring at the terminal end as shown in Fig. 28.

That is, an improved example for the enlarged anchor wirings 32 are shown in Fig. 28.

(1) An enlarged anchor wiring 32 is connected to a bump land 12 to an opposing wiring 11.

(2) Enlarged anchor wiring 32 is extended longitudinally in a vacant space of the wirings 11.

(3) Enlarged anchor wiring 32 is extended laterally in the vacant space of the wirings 11.

(4) Adjacent extended anchor wirings 32 are connected with each other. In each of the examples, the cutting performance of the notch 27 can be stabilized by the increase of the adhesion strength between the wiring 10 and the tape 9 by increasing the effective area for the portion of the enlarged anchor wirings 32.

8. Wide elastomer structure

In the technical explanation for the wide elastomer structure, Fig. 29 is a perspective view illustrating a structure of a standard elastomer, Fig. 30 is a perspective view illustrating the state of appending a semiconductor chip in a standard elastomer, Fig. 31 is a perspective view illustrating the structure of a wide elastomer, Fig. 32 is a perspective view illustrating the state of appending a semiconductor chip in the wide elastomer and Fig. 33 is a cross sectional view illustrating the state of appending a semiconductor chip in the wide elastomer.

In the technique studied by the present inventor, the elastomer 2 is bonded being bisected on both sides of a bonding pad 7 of a semiconductor chip 1 and, in a structure using a standard elastomer 33 as shown in Fig. 29 and Fig. 30, it is considered that warping occurs in the flexible wiring substrate undergoing the effect of peripheral protrusions in a structure in which the surface of the elastomer 2 is smaller than that of the semiconductor chip 1 as shown in Fig. 13 and that the warping brings about a problem, for example, upon forming the solder bumps 5 and mounting of the substrate.

On the contrary, in the structure of a wide elastomer 34 greater than the outer shape of the semiconductor chip 1 of the embodiment as shown in Fig. 31, the peripheral pro-

trusions of the wide elastomer 34 are out of the semiconductor chip as shown in Fig. 32 and Fig. 33 after appending the semiconductor chip. 1 and since the semiconductor chip 1 is bonded substantially to a flat portion of the wide elastomer 34, warping of the flexible wiring substrate 3 can be suppressed.

Further, as shown in Fig. 33, since a wide coating area of an adhesive 8 can be taken, a portion in which the adhesive 8 is not prevail and left unbonded is reduced, and since the adhesive is bled uniformly to the periphery of the semiconductor chip 1 to form an adhesive bleeding 35, it is possible to constitute a package of excellent moisture proofness and reliability without applying peripheral sealing.

That is, the width of the protrusions at the periphery of the wide elastomer 34 is, for example, about 200 to 300 μm while different depending on the physical property of the material and, accordingly, the wide elastomer 34 is formed over a larger range for the entire circumference at least by more than the protrusion width than the chip size of the semiconductor chip 1 as shown in Fig. 3 in the Embodiment 1.

Further, while the flatness is improved by forming the wide elastomer 34 large enough, if the tape 9 is to be cut just at the outer circumference of the semiconductor chip 1, the tape 9 is cut together with the wide elastomer 34 along

a cutting line 36, and it is necessary to define a package outer shape.

As described above, by using the wide elastomer 34 greater than the outer shape of the semiconductor chip 1, warping of the flexible wiring substrate 3 can be suppressed, and bondability of the semiconductor chip 1 can be made stable to improve the moisture proofness and the reliability of the package.

9. Groove-filling technique of elastomer

In the technical explanation for the groove-filling technique of the elastomer, Fig. 31, Fig. 32 are perspective views illustrating the structure of the wide elastomer and the state of appending the semiconductor chip as described above, Fig. 34 is a perspective view illustrating the structure after appending a semiconductor chip by a standard elastomer, Fig. 35 is a cross sectional view thereof, Fig. 36 is a perspective view illustrating a structure after appending a semiconductor chip by a wide elastomer, Fig. 37 is a cross sectional thereof, Fig. 38 is a cross sectional view illustrating the concept of a metal mask printing, Fig. 39 is a plan view illustrating a metal mask of a standard elastomer, Fig. 40 is a plan view illustrating a metal mask of a wide elastomer, Fig. 41 is a plan view illustrating a printed shape of an wide elastomer having plural suspension

and Fig. 42 is a plan view illustrating a potting position for groove-filling of the wide elastomer.

For example, in the structure of a standard elastomer 33 shown in Fig. 34 and Fig. 35 in the technique studied by the present inventor, when an elastomer 2 is constituted by printing using a metal mask 37 as shown in Fig. 38, in the structure of the standard elastomer 33 shown in Fig. 34 and Fig. 35, since a suspended portion 39 is always present at a printing area opening 38 of the metal mask 37 shown in Fig. 40, a groove 40 (space) surrounded by walls of the semiconductor chip 1 and the elastomer 2 is left below the tape suspended portion.

Accordingly, when the window opening 23 is resin-encapsulated in a structure in which the groove 40 is left in the space defined with the semiconductor chip 1 and the elastomer 2, since the sealant 6 leaks through the groove 40, it is necessary to previously seal the portion by a method such as separate potting and then seal the window opening 23.

As described above, the concept of the printing by the metal mask 37 is to form the elastomer 2 for a desired range to a desired thickness, by positioning and disposing a metal mask 37 having a printing area opening 38 at a predetermined position of a flexible wiring substrate 3 as a printed matter, only to the printed portion as shown in Fig. 39 in

the case of the standard elastomer 33 and as shown in Fig. 40 in the case of the wide elastomer 34.

Accordingly, in the Embodiment 1, the wide elastomer 34 described above shown in Fig. 31 is printed by the metal mask 37 as shown in Fig. 40, in which a groove 40 surrounded by the walls of the semiconductor chip 1 and the elastomer 2 can be narrowed by printing the elastomer 2 having a restricted suspension portion 39 for the printing area opening 38 of the metal mask 37. For example, the minimum value for the width of the groove 40 defined by the strength of the suspension portion 39 of the metal mask 37 is about 200 μm.

Further, in a case of a structure in which the semiconductor chip is appended by coating the adhesive 8 on the main surface of the elastomer 2, if the adhesive 8 is coated in a sufficient amount as shown in Fig. 36 and Fig. 37, an excessive adhesive 8 fill the groove 40 by the pressure upon appending to make the window opening 23 to a closed space, so that the window opening 23 can be sealed without applying sealing.

Further, the groove-fillage can be improved by restricting the suspension portion 39 of the metal mask 37 thereby narrowing the groove 40 but this results in a side effect of lowering the strength of the metal mask 37. Then, by providing a plurality of suspension positions on one side as shown in Fig. 41, the strength of the metal mask 37 can

be improved without changing the width of the groove 40 although the number of the grooves 40 is increased.

Further, with an aim of improving the groove-fillage, as shown in Fig. 42, when resin, adhesive or the like is potted, for example, to the potting position 42 of the groove 40 of the elastomer 2 to form a stopping dam for the sealant flow just before appending the semiconductor chip 1, the groove-fillage can be improved further.

Further, also in a case of filling by potting before sealing the window opening 23 after appending and bonding of the semiconductor chip as in the technique studied above, the sealing performance can be improved outstandingly by restricting the width of the groove 40.

As described above, the groove-fillage can be improved, particularly, by restricting the suspension portion 39 of the metal mask 37 thereby narrowing the groove 40 of the elastomer 2 and, further, the groove-fillage can be improved further by previously forming a stopping dam for the sealant flow to the potting position 42.

10. Inner lead bonding technique

In the explanation for the inner lead bonding technique, Fig. 43 is a cross sectional view illustrating a bonding portion by a standard lead bonding, Fig. 44 is a cross sectional view illustrating a bonding portion by using

a stud bump, Fig. 45 and Fig. 46 are cross sectional view and a plan view illustrating lead connection by using soldering, Fig. 47 and Fig. 48 are cross sectional view and a perspective view illustrating lead connection using solder or Au ball, Fig. 49 is a cross sectional view illustrating connection by using Al or solder wire and Fig. 50 is a cross sectional view illustrating connection using an Au wire.

For example, in the technique studied by the present inventor, a lead 11 on which Au-plating is grown is directly driven to a bonding pad 7 and thermally press bonded by supersonic waves. In this case, if the bonding condition is poor or the shape of the bonding tool 18 is inadequate, it is considered to bring about a problem that the bonding strength is low or the bonding pad for a portion therebelow undergoes damages.

On the contrary, in the Embodiment 1, the problems, for example, of bondability or damages caused by the bonding condition and the shape of the bonding tool 18 described above can be overcome by adopting the following means for the bonding state.

That is, Fig. 44 shows an example of using a stud bump 43. This example has a feature of using a semiconductor chip 1 having the stud bump 43 formed previously by a plating method or a ball bonding method to a bonding pad 7 of the semiconductor chip 1, and the bondability is improved and,

further, damages are prevented by the stud bump 43.

Further, Fig. 45 and Fig. 46 are examples of connection for the lead 11 using a solder 44 showing a connection state of surrounding the lead 11 with the solder 44. This example concerns a technique of a connection structure of connecting a bonding pad 7 comprising Al or the like of the semiconductor chip 1 and an electrode of a tape 9 such as TAB as a CSP substrate. A method of feeding the solder 44 in this example includes a method of connecting the solder 44 with the bonding pad 7 of the semiconductor chip 1 using the tape 9 already in which the solder 44 is already present so as to surround the lead 11.

For the connection method, it is desirable that the shape of the solder 44 provided to the tape 9 such as TAB is made as flat as possible at the surface in contact with the bonding pad 7 of the semiconductor chip 1 in the connection method by pressurizing and heating using a bonder. Further, in a connection method using a reflow furnace, solder paste or flux is present to the surface of the bonding pad 7 of the semiconductor chip 1 so as to be in contact with the solder 44 of the tape 9 such as TAB.

Then, in the case of feeding the solder 44 by using the solder paste, the solder paste is present to the surface of the bonding pad 7 of the semiconductor chip 1 by printing or using a syringe. In this case, the tape 9 such as TAB may

be bonded previously or subsequently providing that the lead 11 of the tape 9 is in contact with the solder 44 when the tape 9 is bonded to the semiconductor chip 1.

Further, Fig. 47, Fig. 48 show a connection technique having a feature of connecting a lead 11 of a tape 9 such as TAB onto a bonding pad 7 of a semiconductor chip 1 by using a stud bump such as a solder or Au ball 45.

Further, Fig. 49 shows an example of connecting a wiring 10 of a flexible wiring substrate 3 and a bonding pad 7 of a semiconductor chip 1 by using an Al or solder wire 46. Further, Fig. 50 shows an example of connecting a wiring 10 of a flexible wiring substrate 3 and a bonding pad 7 of a semiconductor chip 1 by using an Au wire 47. In the connection examples, the connection is enabled not by way of the inner lead bonding such as TAB but under the concept of a usual wire bonding.

11. Lead design technique capable of forming S-shape with no tool return

In the explanation for the lead design technique capable of forming an S-shape with no tool return, Fig. 17 is a cross sectional view illustrating a trace of a bonding tool upon forming a standard S-shaped lead explained previously, Fig. 51 is a perspective view for explaining the lead design, Fig. 52 is a perspective view illustrating deformation of a

lead after bonding. Fig. 53 is an explanatory view illustrating a relationship between a lead size and a bending stress ratio and Fig. 76 to Fig. 80 are cross sectional views illustrating the deformed shape of a lead in accordance with the bending stress ratio.

For instance, as explained also in the technique for the planer S-shaped lead 26 in the technique studied by the present inventor, it is necessary for forming the S-shaped configuration of the lead 11 shown in Fig. 17, to laterally displace the bonding tool 18, namely, a special bonding tool trace 25 including tool return is required.

On the contrary, in the Embodiment 1, if the size of a lead 11 shown in 51 is defined, for example, as shown in Fig. 53, the bending stress ratio α is within a desired range of from 1.2 to 1.5 and a suitable S-shaped configuration for the lead 11 as shown in Fig. 52 can be formed by merely driving down the bonding tool 18 vertically with no tool return. In Fig. 52, are shown a tape end 48, a corner 49 on the side of the tape and a corner 50 on the side of the chip.

For example, in the example of embodiment (1), the bending stress ratio α = 1.26 at the size: taper length L1 = 100 μm, wiring length L2 = 380 μm, taper width b1 = 65 μm, lead width b2 = 38 μm and lead thickness h = 18 μm. In the same manner, the ratio is 1.25 in the embodiment (2), 1.26 in the embodiment (3), 1.31 in the embodiment (4) and

1.46 in the embodiment (5).

On the contrary, in the studied technique, at the size: taper length L1 = 100 μm, wiring length L2 = 280 μm, taper width b1 = 60 μm, lead width b2 = 38 μm and lead thickness h = 18 μm, the bending stress ratio α is 1.02, for example, in the example (1) and 1.13 example (2) which is out of the range of 1.2 to 1.5.

As described above, since the bending stress is concentrated to an intermediate portion of the lead 11 upon wiring operation within the range of the bending stress ratio α from 1.2 to 1.5, a moderately distorted satisfactory wiring state is attained. On the other hand, if the bending stress ratio α is less than 1.2 as in the studied technique, since the bending stress is concentrated to the tape end 48 of the lead 11, it results in a stiffened state. Further, if the ratio exceeds 1.5, the bending stress is concentrated only to the intermediate portion of the lead 11 to result in a state of a small radius of curvature which can not be said to be a satisfactory wiring state.

Then, Fig. 76 to Fig. 80 show the deformed shape of the lead in accordance with the bending stress ratio α concretely. At first, when the bonding tool 18 is merely driven down vertically to the lead of the initial shape before wiring shown in Fig. 76, since the bending stress is concentrated to the tape end 48 of the lead 11, for example, in the

wiring operation at $\alpha < 0.9$, an extremely stiffened wiring state is formed as shown in Fig. 77. Accordingly, since high repeating stresses are exerted on the lead 11 during temperature cycle after wiring, the fatigue life is extremely shortened.

Further, since the bending stress is concentrated to the tape end 48 of the lead 11 in the wiring operation at $0.9 \leqq \alpha < 1.2$ as in the technique studied by the present inventor, a somewhat stiffened wiring state is formed as shown in Fig. 78. Accordingly, since high repeating stressed are exerted on the lead 11 during temperature cycle after the wiring, fatigue life is shortened.

On the contrary, since the bending stress is concentrated to an intermediate portion of the lead 11 during wiring operation at $1.2 \leqq \alpha \leqq 1.5$ as in the Embodiment 1, a moderately distorted wiring state as shown in Fig. 79 is formed. Accordingly, since no high repeating stresses are exerted on the lead 11 during temperature cycle after the wiring, the fatigue life is increased.

Further, upon wiring operation at $1.5 < \alpha$ with increased bending stress ratio, since the bending ratio is concentrated only at the intermediate portion of the lead 11, a wiring state with a small radius of curvature as shown in Fig. 80 is formed. Accordingly, since the initial strength of the bent portion is lowered, the fatigue life

during temperature cycle after wiring is shortened.

As a result, an optimal wiring state with the moderately distorted wiring shape is formed when the bending stress ratio is set within a range: $1.2 \leqq \alpha \leqq 1.5$ as in the Embodiment 1, and the temperature cycle life of the lead 11 can be increased.

The bending stress ratio α is defined as a value formed by dividing the stress $\sigma 1$ generated at the corner 49 of the lead 11 on the side of the tape by a stress $\sigma 0$ generated at the tape end 48 of the lead 11 upon conducting the operation of raising the lead 11 just above the bonding pad 7 by the bonding tool 18. That is, the bending stress ratio α can be represented by the following formula based on the size of the lead 11 having a feature in the tapered shape:

$$\alpha = \sigma 1/\sigma 0 = b1 \times (L2 - L1)/(b2 \times L2)$$

As described above, when the size and the shape of the lead 11 are designed such that the bending stress ratio α is from 1.2 to 1.5, stable and suitable S-shaped wiring state can be formed by a simple driving down trace of a wire bonder like that in the technique for the planer S-shaped lead 26 described above. Accordingly, since no special soft-modified wire bonder is required and the bonding tool trade 25 can also be simplified, an effect of shortening the tact time upon bonding can also be expected.

12. Ni-platingless lead

In the technical explanation for the Ni-platingless lead, Fig. 54 is a cross sectional view illustrating a connection portion for the lead connection, Fig. 55 is an enlarged cross sectional view illustrating a bent portion of a lead, Fig. 56 is an enlarge cross sectional view illustrating a bent portion of an Ni-platingless lead, Fig. 57 is an enlarged cross sectional view illustrating a press contact portion of a lead and Fig. 58 is an enlarged cross sectional view illustrating a press-contact portion of the Ni-platingless lead.

For example, in the technique studied by the present inventor, in a case of a cross sectional structure of a lead 11 in which Ni-plating is applied to a surface and an Au plating is applied further to the surface as a Cu core lead instead of a pure Au lead, since the Ni-plating layer is hard and brittle, if it is intended to obtain the S-shaped lead configuration, it is considered to result in a problem of causing crack 51 at the bent portion of the lead 11 as shown in Fig. 55, or a bonding pad 7 or a portion therebelow suffers from a damage 52 as shown in Fig. 57. The Ni-plating is formed as a barrier layer for preventing Cu atoms from diffusing to the Au plating-surface.

On the contrary, in the Embodiment 1, since both the

hardness and the brittleness are reduced by using an Ni-platingless lead 11 in order to obtain the S-shaped configuration, the crack 51 is less formed to the lead per se and, in addition, the damage 52 to the semiconductor chip 1 as the counter-bonding face can also be moderated.

That is, in the connection state of the lead 11 as shown in Fig. 54, in the lead having a constitution of Cu core 53 + Ni plating 54 + Au plating 55 as shown in Fig. 55 as an enlarged portion A in Fig. 54, the crack 51 is liable to be caused as the radius of curvature in the bent portion is smaller. On the other hand, if the surface of the lead 11 is free from the Ni plating 54 and, for example, formed only with the Au plating 55 as shown in Fig. 56, the crack 51 is less formed to the bent portion of the lead 11 even if the radius of curvature is identical with that in Fig. 55.

Further, also in a press-contact portion of a lead 11 in Fig. 57 illustrating an enlarged portion B in Fig. 54, the lead 11 of a constitution comprising: Cu core 53 + Ni plating 54' + Au plating 55, a damage 52 is liable to be caused at the periphery of a bonding pad 7. On the other hand, if the surface of the lead 11 is free from the Ni plating 54 and, for example, formed only with the Au plating 55 as shown in Fig. 58, the damage 52 is less caused even in a case of bonding under the same lead bonding condition.

As described above, it is possible to suppress the

occurrence of the crack 51 to the lead 11 and moderate the damage 52 to the semiconductor chip 1 while obtaining the S-shaped configuration, by constituting the lead 11 such that only the plating layer, for example, an Au plating is formed to the core material of the Cu core 53.

Therefore, according to the semiconductor integrated circuit device in the Embodiment 1, excellent effects can be obtained as already explained successively by comparison with the package structure studied by the present inventor, in the CSP package technique of substantially the identical size with that of the semiconductor chip, in each of the technical items, namely, 1. Surface wiring structure, 2. Eave optimization of the tape to the elastomer, 3. Optimization of outer shape size of the package, 4. Planer S-shaped lead, 5. Beam lead, 6. Peripheral PIQ size of bonding pad, 7. Improvement of anchor wiring, 8. Wide elastomer structure, 9. Elastomer groove-fillage technique, 10. Inner lead bonding technique, 11. Lead design technique capable of forming S-shaped configuration with no tool return and 12. NI-plating-less lead.

In the Embodiment 1, although explanations have been made for the drawings and the contents of the technique on the premise of the surface wiring structure, the technical items 2 to 12 are not limited to the surface wiring structure but the technique is applicable also to general package

structures such as rear face wiring structure. Accordingly, it can be expected to obtain the same effect as explained on every items when the invention is applied to the general package structure.

The package structure of the Embodiment 1 (Fig. 1, Fig. 2) is shown to a case in which the elastomer 2 is greater than the outer shape of the semiconductor chip 1. In a case where the elastomer 2 is smaller than the outer shape of the semiconductor chip 1 as shown in Fig. 81, improvement for the moisture proofness or the like can be obtained by forming a package structure in which the lateral sides of the semiconductor chip 1 and the elastomer 2 are covered with the sealant 6.

Embodiment 2

Fig. 59 and Fig. 60 are a cross sectional view and a perspective view illustrating a rear face wiring solder resist structure in the semiconductor integrated circuit device of Embodiment 2 according to the present invention.

The semiconductor integrated circuit device of the Embodiment 2 is a ball grid array type semiconductor package like that the Embodiment 1, and it is different from the Embodiment 1 in that this is a technique not based on the surface wiring technique but a technique based on and for improving a rear face wiring structure. For instance, as

shown in Fig. 59 and Fig. 60, in a structure comprising an elastomer 2 (elastic structural material) bonded on a main surface of a semiconductor chip 1 and a flexible wiring substrate 3 (wiring substrate) bonded to a main surface of the elastomer 2, a solder resist 56 (insulation film) is formed on the rear face of the flexible wiring substrate 3.

That is, the flexible wiring substrate 3 comprises a tape 9 (substrate base material) as a base material for the flexible wiring substrate 3 and wirings 10 bonded to the rear face of the tape 9 in which the rear face of the wiring 10 is bonded by way of the solder resist 56 to the elastomer 2. The solder resist 56 is composed of an insulation material such as a light sensitive epoxy resin like that in the Embodiment 1.

The feature of the package structure of the semiconductor integrated circuit device in the Embodiment 2 will be explained including the structure and the process in comparison with the package structure as the technique studied by the present inventor.

For instance, in the rear face wiring structure shown in Fig. 7, in the Embodiment 1 as the technique studied by the present inventor, since the elastomer 2 is formed directly on the main surface of the wirings 10 of the flexible wiring substrate 3, low molecular weight ingredients of the elastomer 3 bleed directly to the lead 11 and if they bleed as far as

the bonding point of the lead 11, it results in a problem of extremely deteriorating the bondability (wire bonding stress) by the contamination.

Further, compared with the direct plating surface of the read 11, the surface of the tape 9 in which the wirings 10 are etched out between the leads 11 suffers from violent bleeding since the surface of the tape 9 is roughened also with an aim of improving the bondability between the tape 9 and the wirings 10, bleeding tends to be most violent at the edge portion of the lead 1 together with the effect of the surface tension.

Further, in the rear face wiring structure in which the elastomer 2 is formed to an uneven surface of the wirings 10 caused between the portions with or without the wirings 10, voids are liable to be left, for example, in the gap between the wirings which may cause a worry in view of the reliability.

On the contrary, in the Embodiment 2, since the solder resist 56 is formed on the wirings 10 after forming the wirings 10 in the manufacturing step for the flexible wiring substrate 3, direct contact of the elastomer 2 with the wirings 10 can be prevented. In the same manner, contact of the elastomer 2 to the roughened surface of the tape 9 can also be prevented. This can suppress bleeding of the low molecular weight ingredients of the elastomer 2.

Further, by coating the solder resist 56 to the uneven

surface of the wirings 10 of the flexible wiring substrate. the surface of the wirings 10 is flattened to avoid a disadvantage such as involving of voids upon forming the elastomer 2.

Accordingly, in the semiconductor integrated circuit device of the Embodiment 2, since the solder resist 56 is formed on the wirings 10 of the flexible wiring substrate 3 in the CSP semiconductor package technique based on the rear face wiring structure, it is possible to prevent the lowering of the bondability while preventing contamination to the lead 11 and can obtain a package structure of high reliability with no voids.

Embodiment 3

Fig. 61 is a plan view of a semiconductor integrated circuit device as an Embodiment 3 according to the present invention, as viewed from the rear face of a semiconductor chip, Fig. 62 is a plan view, Fig. 63 is a cross sectional view, Fig. 63 is an enlarged cross sectional view for portion A in Fig. 63 and Fig. 65 is a plan view for a explaining the wiring structure of the wiring substrate.

A semiconductor integrated circuit device in the Embodiment 3 adopts, instead of the semiconductor package of the structure in which the bonding pad is formed about at the center of the chip as in the Embodiments 1 and 2 described

above, a packaging structure of using a semiconductor chip 1a in which a pad is formed to the periphery of the chip as shown in Fig. 61 to Fig. 65 and in which bumps 5a connected to the bonding pads to the semiconductor chip 1a are disposed to a region inward of the outer circumference of the semiconductor chip 1a. The Embodiment 3 also has a structure of adopting the techniques from "1. Surface wiring structure" to "12. Ni-platingless lead", as well as the technical features for each of the technical items for the rear face wiring solder resist structure as explained in the Embodiment 2.

That is, the semiconductor integrated circuit device in the Embodiment 3 is, for example, a 24 pin ball grid array type semiconductor package structure, in which an elastomer 2a (elastic structural material), a flexible wiring substrate 3a (wiring substrate) having wirings 10a formed on a tape 9a and a solder resist 4a (insulation film) are disposed on a main surface of a semiconductor chip 1a formed with a plurality of bonding pads 7a (external terminals), solder bumps 5a (bump electrodes) are formed to an opening of the solder resist 4a, and a portion for forming the bonding pads 7a and lateral sides of the elastomer 2a and the flexible wiring substrate 3a are covered with a sealant 6a.

The semiconductor chip 1a has a peripheral pad structure, for example, as shown in Fig. 65, in which a plurality of bonding pads 7a are formed being arranged in a square pattern

along the outer circumference of the semiconductor chip 1a. The bonding pad 7a of the semiconductor chip 1a is connected electrically with the solder bump 5a by way of the wiring 10a of the flexible wiring substrate 3a which is connected at one end of the lead 11a to the pad 7a and joined at the bump land 12a at the other end of the wiring 10a to the bump 5a. The solder bumps 5a are disposed being arranged as 6 row x 4 column in a region inward to the arrangement for the bonding pads 7a.

Accordingly, also in the semiconductor integrated circuit device of the Embodiment 3, excellent effects can be obtained for each of the technical items as explained for the Embodiments 1 and 2 although there is a difference in the semiconductor package structure as the fan-in peripheral pads. Particularly, in the fan-in package structure, a CSP structure package about at the same size as the semiconductor chip 1a can be attained like that in the Embodiments 1 and 2.

Embodiment 4

Fig. 66 is a plan view of a semiconductor integrated circuit device as an Embodiment 4 of the present invention as viewed from the rear face of the semiconductor chip, Fig. 67 is a plan view, Fig. 68 is a cross sectional view, Fig. 69 is an enlarged cross sectional view illustrating a portion A in Fig. 68 and Fig. 70 is a plan view for explaining the

wiring structure of a wiring substrate.

The semiconductor integrated circuit device of the Embodiment 4 adopts, instead of the semiconductor package of the structure in which the bump electrodes are disposed in the chip area as in the Embodiments 1 and 2, a package structure of using a semiconductor chip 1b of a peripheral pad structure as shown in Fig. 66 to Fig. 70, in which bumps 5b connected to the bonding pads of the semiconductor chip 1b are disposed to a region outward to the outer circumference of the semiconductor chip 1b. This Embodiment 4 also has a structure of adopting the technique from "1. Surface wiring structure" to "12. Ni-platingless lead", as explained in the Embodiment 1, as well as the features for each of the technical items of the rear face wiring solder resist structure explained for the Embodiment 2 respectively.

That is, the semiconductor integrated circuit device in the Embodiment 4 is, for example, in a 80 pin ball grid array type semiconductor type package structure in which an elastomer 2b (elastic structural material), a flexible wiring substrate 3b (wiring substrate) having wirings 10b formed on a tape 9b, and a solder resist 4b (insulation film) are disposed on a main surface of a semiconductor chip 1b formed with a plurality of bonding pads 7b (external terminals), solder bumps 5b (bump electrodes) are formed to an opening portion of the solder resist 4b, portions for forming bonding pads 7b are

covered with the sealant 6b, and a support ring 57b is disposed to the lateral side of the semiconductor chip 1b to constitute a package structure.

The semiconductor chip 1b has a peripheral pad structure, for example, as shown in Fig. 70, and a plurality of bonding pads 7b are formed being arranged in a square pattern along the outer circumference of the semiconductor chip 1b. The bonding pad 7b of the semiconductor chip 1b is connected electrically with the solder bump 5b by way of the wiring 10b of the flexible wiring substrate 3b which is connected at one end of the lead 11b with the pad 7b and joined at the bump land 12b at the other end with the bump 5b. The solder bumps 5b are disposed by being arranged in two rows in a square pattern to a resin outward to the arrangement of the bonding pads 7b of the semiconductor chip 1b.

Accordingly, the semiconductor integrated circuit device of the embodiment 4 can also obtain excellent effects for each of the technical items as explained for the Embodiments 1 and 2 although having a difference as a semiconductor package structure of fan-out peripheral pad. Particularly, the fan-out package structure can provide a package structure corresponding to multi-pin arrangements although the size of the semiconductor package is increased compared with the Embodiments 1 and 2.

Embodiment 5

Fig. 71 is a plan view of a semiconductor integrated circuit device as an Embodiment 5 of the present invention as viewed from the rear face of the semiconductor chip, Fig. 72 is a plan view, Fig. 73 is a cross sectional view, Fig. 74 is an enlarged cross sectional view illustrating a portion A in Fig. 73 and Fig. 75 is a plan view for explaining the wiring structure of a wiring substrate. In Fig. 75, a portion such as the number of bonding pads and solder bumps are omitted for simplification in order to make the arrangement of wirings clearer.

The semiconductor integrated circuit device of the Embodiment 5 adopts, instead of the semiconductor package of the structure in which bump electrodes are disposed in the area of the chip as in the Embodiments 1 and 2, a package structure of using a peripheral pad structure semiconductor chip 1c as shown in Fig. 71 to Fig. 75, in which solder bumps 5c connected to the bonding pads of the semiconductor chip 1c are disposed both in inner and outer regions to the semiconductor chip 1c. This Embodiment 5 also has a structure adopting the technique from "1. Surface wiring" to "12. Ni-platingless lead" as explained for the Embodiment 1, as well as features for each of the technical items of the rear face wiring solder resist structure as explained for the Embodiment 2.

That is, the semiconductor integrated circuit device in the Embodiment 5 is, for example, a 110 pin ball grid array type semiconductor package structure in which an elastomer 2c (elastic structural material), a flexible wiring substrate 3c (wiring substrate) having wirings 10c formed on a tape 9c, and a solder resist 4c (insulation film) on a main surface of a semiconductor chip 1c formed with a plurality of bonding pads 7c (external terminals), solder bumps 5c (bump electrodes) are formed to an opening portion of the solder resist 4c, a portion of forming the bonding pads 7c is covered with a sealant 6c and a support ring 57c is disposed to the lateral sides of the semiconductor chip 1c.

The semiconductor chip 1c has a peripheral pad structure, for example, as shown in Fig. 75 (actual arrangement in Fig. 72) in which a plurality of bonding pads 7c are formed by being arranged in a square pattern along the outer circumference of the semiconductor chip 1c. The bonding pad 7c of the semiconductor chip 1c is electrically connected to the solder bump 5c by way of the wiring 10c of the flexible wiring substrate 3c that is connected by a lead 11c at one end to the pad 7c and joined to the bump 5c at the bump land 12c at the other end of the wiring 10c. The solder bumps 5c are arranged as 6 row x 5 column in a region inward of the arrangement of the bonding pads 7c of the semiconductor chip 1c, and disposed by being arranged in two rows in a square

pattern also in the outer region.

Accordingly, the semiconductor integrated circuit device of the Embodiment 5 can also obtain similar excellent effect in each of the technical items as explained for the Embodiments 1 and 2 although there is a difference as the semiconductor package structure. Particularly, in the fan-in/out package structure, a package structure capable of coping with multi-pin arrangements can be adopted although the size of the semiconductor package is enlarged compared with the Embodiments 1 and 2.

While the invention made by the present inventor has been explained with reference to the Embodiments 1 - 5 of the invention, the present invention is not restricted only to those embodiments but it will be apparent that various modifications are possible within a range as not departing the gist thereof.

For example, the techniques in the Embodiments 1 - 5 can be combined as required.

The number of the solder bumps as the external connection terminals of the semiconductor package and the bonding pads as the external terminals of the semiconductor chip electrically connected with the solder bumps are not restricted only to those explained in the embodiments, but they may be properly modified depending on or in accordance with the specification of the packages such as integrated

circuits formed on the semiconductor chip.

Further, regarding the materials, for example, for the elastomer as the elastic structural material, the tape for the flexible wiring substrate as the wiring substrate, the wiring and lead plating, the solder resist as the insulation film and the solder bump as the bump electrode, the invention is also applicable in a case of using other materials having respective properties.

For example, as the solder resist, there can be mentioned a resin mixture comprising an acrylic resin and an epoxy resin, the resin mixture described above with addition of a filler, melamine, acryl, polystyrol and polyimide, as well as polyurethane and silicone and it is necessary that they have a property of withstanding the soldering temperature and resistance to the exposure of flux and cleaning solvent.

Advantageous effects obtained by typical examples among those disclosed in the present invention are briefly explained below.

(1) Since the elastic structural material is disposed on the flat surface on the rear face of the substrate base material by adopting the surface wiring structure in which the elastic structural material is disposed on the rear face of the substrate base material of the wiring substrate, and the insulation film is formed on the main surface of the wirings formed on the main surface of the substrate base

material, the elastic structural material can be mounted at a higher accuracy and stably to the substrate base material in a voidless manner and, since the size and the shape of the elastic structural material are made stable, the bonding step for the semiconductor chip is also stable thereby enabling assembling at higher yield.

(2) Since the signal wiring layer and the power source ground wiring layer can be separated into different layers by making the wirings of the wiring substrate into a multi-wiring layer structure, excellent electric characteristic in view of the noise resistance can be attained.

(3) Since external terminals of the semiconductor chip can be disposed at the central portion or the peripheral portion, and the bump electrodes connected to the external terminals can be disposed to the inside, outside or both of the regions outward to the outer circumference of the semiconductor chip, it is applicable to package structures of various types and variations.

(4) Since the eave of the substrate base material can be optimized relative to the elastic structural material by setting the size between the end of the elastic structural material of the semiconductor chip on the side of the external terminals and the end of the substrate base material of the wirings substrate based on the ingredients of the elastic structural material, variation in the height of the

bump electrodes is not caused, it is free from the difficulty for filling the sealant caused by the enlarged sealing region for the opening of the elastic structural material an it is possible to prevent contamination of wirings caused by the bleeding ingredients or evaporative ingredients of the elastic structural material.

(5) Since the outer shape size of the package can be optimized by setting the relation for the distance M2 between the end of the substrate base material of the wiring substrate and the end of the elastic structural material and for the distance M1 between the end of the semiconductor chip and the end of the substrate base material at the outer circumference of the semiconductor integrated circuit device within a range: $M1 > M2 > 0$, the outermost circumference of the package is not of the semiconductor chip, so that a possibility of inducing chip cracks is reduced during assembling step, withdrawal and insertion of receptacles and tray transportation, and the circuit surface of the semiconductor chip is not exposed to the outside thereby enabling to improve the reliability. Further, since the peripheral protrusions of the elastic structural material after printing do not interfere with the bonding portion of the semiconductor chip, it is possible to prevent bonding failure upon appending, worsening of the flatness of the wiring substrate and lowering of the reliability.

(6) Since the planer S-shaped wiring can be obtained by forming the wiring of the wiring substrate such that the fixed portion with the substrate base material and top end portion connected to the external terminal of the semiconductor chip are displaced at least by more than the width of the wiring, a stable and suitable S-shaped lead can be formed because a sag due to the original planer S-shaped configuration can be obtained by a simple driving down trace of a usual wire bonder, so that a stable S-shaped configuration can be formed for the lead with no requirement of a soft-modified special wire bonder and further the tact time upon bonding can also be shortened since the bonding tool trace can also be simplified.

(7) Since the beam wiring can be attained by forming the wiring of the wiring substrate as a cantilever structure which is fixed at one end to the substrate base material, it is possible to overcome such problems as in notched wirings that cutting is impossible upon bonding due to the variation of the size of the notches and, even if it can be cut, it may be cut at a portion different from the desired notch, or it is cut before plating step for the wiring substrate because of the excessively narrowed portion, failing to deposit plating.

(8) Since the end of the opening of the surface protection film on the semiconductor chip is set to a size within such

a range as the wiring does not interfere with the surface protection film when the bonding tool is driven down, it is possible to overcome the problem that the surface protection film or the semiconductor chip suffers from damages (on the semiconductor chip) by the driving down, and the ingredients of the surface protection film are deposited to the bonding portion on the lower surface of the lead to cause contamination and worsen the bondability.

(9) Since the effective area of the wired portion can be enlarged by connecting the wiring on the notch terminal end of the wiring substrate to an opposing land portion of the wiring, longitudinally or laterally extending the wiring in the vacant regions of the wirings or connecting the adjacent wirings to each other, it is possible to increase the bonding strength between the wiring and the substrate base material and obtain stable notch cutting performance.

(10) Since the wide elastic structural material structure can be attained by forming the elastic structural material in a larger range over the entire circumference at least by more than the with of the protrusions on the outer circumference formed to the elastic structural material as compared with the outer shape size of the semiconductor chip, protrusions on the periphery of the elastic structural member are out of the semiconductor chip after the appending the semiconductor chip and it is bonded substantially on the flat

portion of the elastic structural material, the warping of the wiring substrate is suppressed. Further, since a large coating area for the adhesive can be taken a not bonded portion caused by the insufficient prevailing of the adhesive is less formed and the adhesive bleeds out uniformly to the periphery of the semiconductor chip, so that a package of excellent moisture proofness and reliability can be constituted with out applying peripheral sealing.

(11) In a case of forming the elastic structural material being divided such that it is not bonded on the external terminals of the semiconductor chip, when each of the end of the spaces at which the divided elastic structural materials are opposed is formed as a grooved shape, the metal mask suspension portion can be restricted to narrow the groove of the elastic structural material in the groove-fillage technique of the elastic structural material, so that the groove-fillage of the elastic structural material can be improved.

(12) If a plurality of grooves are formed to each of the ends of the elastic structural material, the strength of the groove-forming metal mask can be improved.

(13) When a stopping dam for sealant flow is previously formed to the grooves at each of the ends of the spaces at which the divided structural materials are opposed, the groove-fillage in the sealing step can further be improved.

(14) By previously forming stud bumps to the external

terminals of the semiconductor chip and connecting the external terminals of the semiconductor chip and the wirings of the wiring substrate by way of the stud bumps, problems for the bondability and damages can be solved in the inner lead bonding technique, the bondability is improved by the stud bumps and, further, damages can be prevented.

(15) By supplying the solder so as to previously surround the wirings of the wiring substrate and connecting the external terminals of the semiconductor chip and the external terminals of the semiconductor chip by way of the solder, bondability can be improved and damages can be suppressed in the bonding technique.

(16) By using the stud bumps, for example, made of solder or Au so as to surround from above the wirings of the wiring substrate and connecting the wirings of the wiring substrate and the external terminals of the semiconductor chip by way of the stud bumps, the bondability can be improved and the damages can be suppressed in the bonding technique.

(17) By connecting the wirings of the wiring substrate and the external terminals of the semiconductor chip by using an Al, solder or Au wire, the problem, for example, of bondability or damages can be solved and it is possible to attain connection by the concept of a usual wire bonding not by the inner lead bonding such as TAB.

(18) By forming the lateral size of the wiring of the

wiring substrate such that the size is gradually narrowed from the end of the substrate base material of the wiring substrate to the top end of the wiring and the lateral size is made constant from a predetermined position, and setting the size and the shape of the wiring such that the bending stress ratio α is from 1.2 to 1.5, since a suitable S-shaped configuration can be formed by merely driving down the bonding tool vertically with no return of the bonding tool, a lead of a stably shaped configuration can be formed without requiring a special soft-modified wire bonder and, further, the tact time upon bonding can also be shortened since the trace of the bonding tool can be simplified.

(19) By using the electroconductive material as a core material for the wiring structure of the wiring substrate and applying only Au plating to the surface, since both the hardness and the brittleness of the lead are lowered as compared with a case of applying Ni-plating between the core material of the conductive material such as Cu and Au plating, cracks are less caused to the lead itself, as well as damages to the semiconductor chip as the counter bonding face can also be moderated.

(20) By forming the wirings on the rear face of the substrate base material of the wiring substrate, forming the insulation film on the rear face of the wirings and disposing the elastic structure material on the rear face of

the insulation film, since the rear face wiring insulation film structure can be obtained, direct contact of the elastic structural material with the wiring can be prevented and contact of the elastic structural material to the roughened the surface of the substrate base material can also be prevented, so that bleeding of the low molecular weight ingredients of the elastic structure material can be suppressed and, further, the surface of the uneven wiring surface can be flattened by coating the insulation film making it possible to avoid disadvantages such as involving of voids upon forming the elastic structural material.

(21) In the surface wiring structure, since the opening of the insulation film is formed by defining the coating range of the insulation film material, the fabrication accuracy for the hole diameter can further be improved as compared with a case of forming the opening by machining to the substrate base material of the wiring substrate of the rear face wiring structure.

(22) By setting the thickness of the insulation film by determining the coating condition for the insulation film material in the surface wiring structure, since the film can be coated stably at a further reduced thickness and the bump land disposed at a higher density with a small diameter can be formed as compared with the substrate base material, smaller bump electrode can be joined more satisfactorily.

(23) In the surface wiring structure, since the pitch for the arrangement of the bump electrodes can be reduced as compared with the rear face wiring structure, it is possible to constitute a semiconductor package having output terminals at higher density.

CLAIMS :

1. A semiconductor device comprising:

a semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed in a main surface thereof;

an elastic layer formed on the main surface of the semiconductor chip to expose the plurality of external terminals;

an insulating tape formed on the elastic layer and having an opening to expose the plurality of external terminals, the opening being defined by an edge of the insulating tape;

a plurality of leads formed on a surface of the insulating tape, each of the plurality of leads having a first portion disposed on the insulating tape and a second portion which extends across the edge of the insulating tape and is in the opening of the insulating tape, each of the second portions being electrically connected with a corresponding external terminal of the external terminals; and

a plurality of bump electrodes formed on the first portions of the plurality of leads and being electrically connected to the plurality of leads,

wherein each of the plurality of leads includes copper lead as core material,

wherein each of the plurality of leads has gold-plating which is directly performed to a surface of the copper lead, and

wherein a length of the second portion of each of the plurality of leads is longer than a straight line distance from the edge of the insulating tape to the corresponding external terminal of the external terminals.

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2. A semiconductor device according to claim 1, wherein any another metallic material does not exist between the copper lead and the gold-plating.

3. A semiconductor device according to claim 1, wherein the plurality of leads are disposed between the elastic layer and the insulating tape, and wherein the plurality of bump electrodes are contacted with the corresponding leads of the plurality of leads respectively via through holes formed in the insulating tape.

4. A semiconductor device according to claim 1, wherein each of the plurality of leads is a substantially straight line form in a plane view and is bended in a sectional view.

5. A semiconductor device comprising;

a semiconductor chip having a plurality of external terminals,

a wiring substrate having a plurality of wirings and a plurality of broad wiring portions, the wiring substrate positioned over the semiconductor chip,

an opening formed in the wiring substrate positioned over the plurality of external terminals,

a first group of plurality of leads projecting inward of the opening, connecting the external terminals,

a second group of plurality of leads projecting inward of the opening, not connecting the external terminals in the opening,

wherein the first and second group of plurality of leads are connecting respectively with the plurality of broad wiring portions via the plurality of wirings,

the plurality of broad wiring portions are wider than the

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plurality of wirings and the first and second group of plurality of leads.

6. A semiconductor device according to claim 5, further comprising an elastic layer positioned between the wiring substrate and the semiconductor chip,

an opening in the elastic layer positioned over the external terminals.

7. A semiconductor device according to claim 5, further comprising a plurality of bump electrodes positioned respectively on a plurality of broad wiring portions connecting respectively with the first group of plurality of leads via the plurality of wirings.

8. A semiconductor device according to claim 5, further comprising a plurality of bump electrodes positioned respectively on the plurality of broad wiring portions.

9. A semiconductor device according to claim 5, wherein a plurality of broad wiring portion connecting respectively with the second group of plurality of leads via the plurality of wirings are further connecting one of the first group of plurality of leads via the plurality of wirings.

10. A semiconductor device according to claim 5, wherein a plurality of broad wiring portion connecting respectively with one of the second group of plurality of leads via the plurality of wirings are further connecting with another one of the second group of plurality of leads.

11. A semiconductor device according to claim 5,

wherein interval pitch of a plurality of broad wiring portion connecting respectively with the first group of plurality of leads via the plurality of wirings is larger than that of the first group of plurality of leads.

12. A semiconductor device according to claim 5, wherein a distance between a plurality of broad wiring portion connecting respectively with the first group of plurality of leads via the plurality of wirings and a edge of opening is different from a distance between a plurality of broad wiring portion connecting respectively with the second group of plurality of leads via the plurality of wirings and a edge of opening.

13. A semiconductor device according to claim 5, wherein the opening having first edge portion and second edge portion opposed to first edge portion,

part of the first group of plurality of leads are protruding from the first edge, and the other part of the first group of plurality of leads are protruding from the second edge.

14. A semiconductor device according to claim 13, wherein part of the second group of plurality of leads are protruding from the first edge, and the other part of the second group of plurality of leads are protruding from the second edge.

15. A semiconductor device according to claim 14, wherein the part of the first group of plurality of leads protruding from the first edge are opposing to the other part of the second group of plurality of leads protruding from the second edge.

the other part of the first group of plurality of leads

protruding from the second edge are opposing to the part of the second group of plurality of leads protruding from the first edge.

16. A semiconductor device comprising;

a semiconductor chip having a plurality of external terminals,

a wiring substrate having a plurality of wirings, a plurality of bump lands, the wiring substrate positioned over the semiconductor chip,

a plurality of bump electrodes positioned on respective bump lands

an elastic layer positioned between the wiring substrate and the semiconductor chip,

an opening formed in the wiring substrate and the elastic layer positioned over the plurality of external terminals,

a first group of plurality of leads projecting inward of the opening, connecting the external terminals,

a second group of plurality of leads projecting inward of the opening, not connecting the external terminals in the opening,

wherein the first and second group of plurality of leads are connecting respectively with the plurality of bump lands via the plurality of wirings,

17. A semiconductor device according to claim 16, wherein the bump lands are wider than the wirings

18. A method of manufacturing a semiconductor device comprising the steps of;

(a) preparing a semiconductor chip having a plurality of semiconductor elements and a row of external terminals on the

main surface,

(b) preparing a wiring substrate having a wiring substrate base, a first array of bump lands, a second array of bump lands, an opening in the wiring substrate base positioned between the first and second array of bump lands, and a plurality of leads respectively connecting between the first array of bump lands and the second array of bump lands, and respectively bridging over the opening,

(c) positioning the wiring substrate over the main surface of the semiconductor chip as the opening is positioned over the row of external terminals

(d) cutting the plurality of leads at the portion over the opening and bonding the plurality of leads on the external terminals respectively through the opening,

19. A method of manufacturing a semiconductor device according to claim 18, further comprising the steps of;

(e) sealing the row of external terminals and the plurality of leads bonded with the external terminals by potting method through the opening.

20. A method of manufacturing a semiconductor device according to claim 18, wherein each of the plurality of leads having a notch at the bridging portion,
in the step of (d), each of the plurality of leads is cut at the notch.

21. A method of manufacturing a semiconductor device according to claim 18, wherein the minimum interval of the external terminals is smaller than the minimum interval of the bump lands.

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22. A method of manufacturing a semiconductor device according to claim 18, in the step of (c), the wiring substrate is positioned over the main surface of the semiconductor chip through an elastic layer.

23. A method of manufacturing a semiconductor device according to claim 18, further comprising a step of;
(e) positioning bump electrodes on each bump lands of the first and second array of bump lands,

24. A method of manufacturing a semiconductor device comprising the steps of;
(a) preparing a semiconductor chip having a plurality of semiconductor elements and a external terminal on the main surface,
(b) preparing a wiring substrate comprising a wiring substrate base, a bump land, an anchor wiring, an opening in the wiring substrate base between the bump land and the anchor wiring, and a lead connecting between the bump land and the anchor wiring and bridging over the opening wherein the anchor wiring is wider than the lead,
(c) positioning the wiring substrate over the main surface of the semiconductor chip as the opening is positioned over the external terminal
(d) cutting the lead at the portion over the opening and bonding the lead on the external terminal through the opening,

25. A method of manufacturing a semiconductor device comprising the steps of;
(a) preparing a semiconductor chip having a plurality of semiconductor elements and a row of external terminals on the main surface,

(b) preparing a wiring substrate comprising a wiring substrate base, a plurality of bump lands, a plurality of anchor wirings, an opening in the wiring substrate base positioned between the plurality of bump lands and the plurality of anchor wirings, and a plurality of leads respectively connecting between the plurality of bump lands and the plurality of anchor wirings, and respectively bridging over the opening, wherein the plurality of anchor wirings are wider than the plurality of leads,

(c) positioning the wiring substrate over the main surface of the semiconductor chip as the opening is positioned over the row of external terminals

(d) cutting the plurality of leads at the portion over the opening and bonding the plurality of leads on the external terminals respectively through the opening,

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