WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a substrate;

a peripheral circuit layer having a transistor provided on the substrate and a first junction metal provided on a first surface; and

a memory cell array layer provided on the first surface including a stacked structure in which a plurality of electrode layers and a plurality of insulating layers are alternately stacked in the first direction, a columnar structure extending in the first direction in the stacked structure and forming a plurality of memory cells at the intersection with the plurality of electrode layers, a first wiring layer provided between the stacked structure and the first surface, a plug electrically connecting one of the plurality of electrode layers with the first wiring layer and extending in the first direction and a second junction metal provided on the first junction metal and electrically connected with the first wiring layer,

wherein the second junction metal overlaps the stacked structure when viewed from the first direction.

2. The semiconductor memory device according to claim 1,

wherein the first junction metal and the second junction metal are directly bonded.

3. The semiconductor memory device according to claim 1, wherein the memory cell array layer comprises:

a second surface in contact with the first surface and a third surface opposite to the second surface,

a second wiring layer provided between the third surface and the laminate,

a third junction metal provided on the third surface electrically connected to the second wiring layer and overlapping the stacked structure when viewed from the first direction, and

a signal line extraction electrode that electrically connecting the first wiring layer and the second wiring layer and extending in the first direction.

4. The semiconductor memory device according to claim 3, further comprising,

a bit line electrically connected to a second surface side of the columnar structure; and

a source line electrically connected to a third surface side of the columnar structure,

wherein the second wiring layer is provided on the third surface side of the source line.

5. The semiconductor memory device according to claim 3 or claim 4, further comprising:

at least one other memory cell array layer of the same type as the memory cell array layer stacked so as to face the memory cell array layer, and having a plurality of memory cell array layers.

6. The semiconductor memory device according to claim 5, further comprising,

a memory string having memory cells storing the ID of each of the plurality of memory cell array layers provided in at least one of the plurality of memory cell array layers,

a transistor provided in at least one of the plurality of memory cell array layers.

7. The semiconductor memory device according to claim 6,

wherein the plurality of memory cell array layers are at least three or more layers, and the transistor provided in one memory cell array layer between another one memory cell array layer and one other memory cell array layer.

8. The semiconductor memory device according to claim 6,

wherein the transistor is provided in each of the plurality of memory cell array layers.