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(US). MITTELBRUNN, Michael, A.; 129 Pembroke
Street, #1, Boston, MA 02118 (US). SABIL, Abdelkebir;
1950 Commonwealth Avenue, Apt. 36, Brighton, MA
02135 (US).

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(74) Agent: RUBENSTEIN, Bruce, D.; Teradyne, Inc., 321
Harrison Avenue, Boston, MA 02118 (US).

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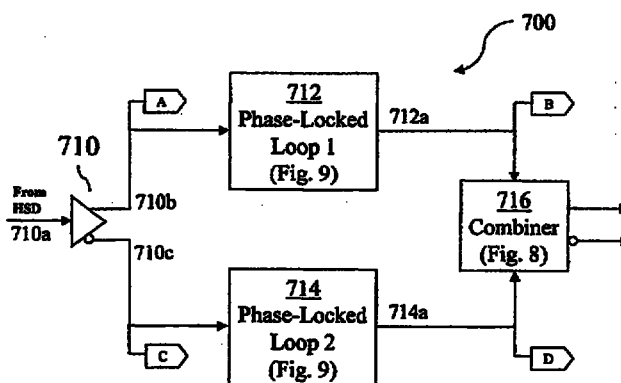
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(71) Applicant: TERADYNE, INC. [US/US]; 321 Harrison
Avenue, Boston, MA 02118 (US).

(72) Inventors: O'BRIEN, David, E.; 19 Queensberry Street,
Apt. 41, Boston, MA 02215 (US). SHEEN, Timothy, W.;
160 Foster Street, Brighton, MA 02135 (US). HUTNER,
Marc, R.; 55 Gore Street, Apt. 3, Cambridge, MA 02141

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(54) Title: LOW JITTER PHASE-LOCKED LOOP WITH DUTY-CYCLE CONTROL



(57) Abstract: A timing circuit (700) for ATE generates an output clock (710a) from an input clock and controls output pulse width. The timing circuit includes a differential driver (710) having an input that receives the input clock, and having inverting and non-inverting outputs. The inverting output is coupled to a first phase-locked loop (712), and the non-inverting output is coupled to a second phase-locked loop (714). The first and second phase-locked loops respectively generate first and second clocks in response to respective rising and falling edges of the input clock. A combiner circuit (716) converts the first and second clocks into narrow pulse trains, and the pulse trains respectively operate SET and RESET inputs of a SET/RESET flip-flop. The SET/RESET flip-flop generates an output clock having rising edges responsive to rising edges of the input clock, and falling edges responsive to falling edges of the input clock. The timing circuit also includes a frequency divider (924) in feedback path of the phase-locked loops, for establishing a frequency gain of the timing circuit. Pulse width of the output clock is based upon pulse width of the input clock and frequency gain of the timing circuit. To promote timing accuracy, the frequency responses of the phase-locked loops are tailored to selectively filter jitter from the input clock that is uncorrelated with jitter in the ATE, but to pass correlated jitter unattenuated.

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