CLAIMS

1. A transistor comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness of less than about 100Å, and the second side having a thickness equal to or greater than 125Å;

wherein the thickness of the second side is at least five times the thickness of the first side.

2. The transistor of claim 1, wherein the thickness of the first side is about 70Å or less.

3. The transistor of claim 1, wherein the thickness of the first side is about 35Å or less.

4. The transistor of claim 1, wherein the source further comprises a third impurity region, the third impurity region being self-aligned.

5. The transistor of claim 4, wherein a maximum doping concentration of the third impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

6. The transistor of claim 4, wherein a doping concentration of the third impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

7. The transistor of claim 6, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

8. The transistor of claim 4, wherein the third impurity region is positioned in a current path of the transistor.

9. The transistor of claim 1, wherein the second side has a thickness of between approximately 120Å and 800Å.

10. The transistor of claim 9, wherein the second side has a thickness of between approximately 200Å and 400Å.

11. The transistor of claim 1, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

12. A transistor comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion
of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than 0.6V;

wherein the transistor is configured as a power switch in a voltage regulator.

13. The transistor of claim 12, wherein the turn-on voltage of the transistor is between 0.4 and 0.5V.

14. The transistor of claim 12, wherein the source further comprises a third impurity region, the third impurity region being self-aligning.

15. The transistor of claim 14, wherein a maximum doping concentration of the third impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

16. The transistor of claim 14, wherein a doping concentration of the third impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

17. The transistor of claim 16, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

18. The transistor of claim 14, wherein the third impurity region is positioned in a current path of the transistor.

19. The transistor of claim 12, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

20. A transistor comprising:

a source region including a first impurity region of a first impurity type implanted into a substrate and a third impurity region of an opposite second impurity type abutting the first impurity region, and a fourth impurity region of the second impurity type surrounding the first impurity region and the third impurity region, the fourth impurity region having a lower doping concentration than the third impurity region;

a drain region including a second impurity region of the first impurity type implanted into the substrate;

an intrinsic diode between the fourth impurity region and the drain region; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

21. The transistor of claim 20, wherein the turn-on voltage of the transistor is between 0.4 and 0.6V.

22. The transistor of claim 20, wherein the fourth impurity region is self-aligning.

23. The transistor of claim 20, wherein a maximum doping concentration of the fourth impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

24. The transistor of claim 20, wherein a doping concentration of the fourth impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

25. The transistor of claim 24, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

26. The transistor of claim 22, wherein the fourth impurity region is positioned in a current path of the transistor.

27. The transistor of claim 20, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

28. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having the source connected to the input terminal and the drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side

formed over a portion of the second impurity region, the first side having a thickness of less than about 100Å, and the second side having a thickness equal to or greater than 125Å;

wherein the thickness of the second side is at least five times the thickness of the first side.

29. The system of claim 28, wherein the thickness of the first side of the oxide layer of the low-side transistor is about 70Å or less.

30. The system of claim 28, wherein the thickness of the first side of the oxide layer of the low-side transistor is about 35Å or less.

31. The system of claim 28, wherein the source region of the low-side transistor further comprises a third impurity region, the third impurity region being self-aligned.

32. The system of claim 31, wherein a maximum doping concentration of the third impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

33. The system of claim 31, wherein a doping concentration of the third impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

34. The system of claim 33, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

35. The system of claim 31, wherein the third impurity region of the low-side transistor is positioned in the current path of the transistor.

36. The system of claim 28, wherein the second side of the oxide layer of the low-side transistor has a thickness between approximately 120Å and 800Å.

37. The system of claim 36, wherein the second side has a thickness of between approximately 200Å and 400Å.

38. The system of claim 28, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

39. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having the source connected to the input terminal and the drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than 0.6V.

40. The system of claim 39, wherein the turn-on voltage of the low-side transistor is between 0.4 and 0.5V.

41. The system of claim 39, wherein the source region of the low-side transistor further comprises a third impurity region, the third impurity region being self-aligning.

42. The system of claim 41, wherein a maximum doping concentration of the third impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

43. The system of claim 41, wherein a doping concentration of the third impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

44. The system of claim 43, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

45. The system of claim 41, wherein the third impurity region of the low-side transistor is positioned in a current path of the transistor.

46. The system of claim 39, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

47. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having the source connected to the input terminal and the drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region of a first impurity type implanted into a substrate, a third impurity region of an opposite second impurity type abutting the first impurity region, and a fourth impurity region surrounding the first impurity region and the third impurity region, the fourth impurity region having a lower doping concentration than the third impurity region;

a drain region including a second impurity region implanted into the substrate;

an intrinsic diode between the fourth impurity region and the drain region; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

48. The system of claim 47, wherein the turn-on voltage of the low-side transistor is between 0.4 and 0.6V.

49. The system of claim 47, wherein the fourth impurity region is self-aligning.

50. The system of claim 47, wherein a maximum doping concentration of the fourth impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

51. The system of claim 47, wherein a doping concentration of the fourth impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

52. The system of claim 51, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

53. The system of claim 47, wherein the fourth impurity region of the low-side transistor is positioned in a current path of the transistor.

54. The system of claim 47, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

CLAIMS

1. A transistor comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is substantially 0.4V;

wherein the transistor is configured as a power switch in a voltage regulator.

2. The transistor of claim 1, wherein the source further comprises a third impurity region, the third impurity region being self-aligning.

3. The transistor of claim 2, wherein a maximum doping concentration of the third impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

4. The transistor of claim 2, wherein a doping concentration of the third impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

5. The transistor of claim 4, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

6. The transistor of claim 2, wherein the third impurity region is positioned in a current path of the transistor.

7. The transistor of claim 1, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

8. A transistor comprising:

a source region including a first impurity region of a first impurity type implanted into a well region, also of the first impurity type, implanted on a substrate and a third impurity region of an opposite second impurity type abutting the first impurity region, and a fourth impurity region of the second impurity type surrounding the first impurity region and the third impurity region, the fourth impurity region having a lower doping concentration than the third impurity region;

a drain region including a second impurity region of the first impurity type implanted into the substrate;

an intrinsic diode between the fourth impurity region and the drain region, the intrinsic diode formed by the fourth impurity region of the second impurity type and the well region of the first impurity type; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

9. The transistor of claim 8, wherein the turn-on voltage of the transistor is between 0.4 and 0.6V.

10. The transistor of claim 8, wherein the fourth impurity region is self-aligning.

11. The transistor of claim 8, wherein a maximum doping concentration of the fourth impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

12. The transistor of claim 8, wherein a doping concentration of the fourth impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

13. The transistor of claim 12, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

14. The transistor of claim 10, wherein the fourth impurity region is positioned in a current path of the transistor.

15. The transistor of claim 8, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

16. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having a source connected to the input terminal and a drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is substantially 0.4V.

17. The system of claim 16, wherein the source region of the low-side transistor further comprises a third impurity region, the third impurity region being self-aligning.

18. The system of claim 17, wherein a maximum doping concentration of the third impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

19. The system of claim 17, wherein a doping concentration of the third impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

20. The system of claim 19, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

21. The system of claim 17, wherein the third impurity region of the low-side transistor is positioned in a current path of the transistor.

22. The system of claim 16, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

23. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having a source connected to the input terminal and a drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region of a first impurity type implanted into a well region, also of the first impurity type, implanted on a substrate, a third impurity region of an opposite second impurity type abutting the first impurity region, and a fourth impurity region surrounding the first impurity region and the third impurity region, the fourth impurity region having a lower doping concentration than the third impurity region;

a drain region including a second impurity region implanted into the substrate;

an intrinsic diode between the fourth impurity region and the drain region, the intrinsic diode formed by the fourth impurity region of the second impurity type and the well region of the first impurity type; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second

side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

24. The system of claim 23, wherein the turn-on voltage of the low-side transistor is between 0.4 and 0.6V.

25. The system of claim 23, wherein the fourth impurity region is self-aligning.

26. The system of claim 23, wherein a maximum doping concentration of the fourth impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

27. The system of claim 23, wherein a doping concentration of the fourth impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

28. The system of claim 27, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

29. The system of claim 23, wherein the fourth impurity region of the low-side transistor is positioned in a current path of the transistor.

30. The system of claim 23, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).