

COMPLIANT PRE-FORM INTERCONNECT

Field of The Invention

The field of the invention is integrated circuit packaging and mounting.

Background of The Invention

5 The use of underfill compositions for mounting integrated circuit (IC) devices supporting surfaces such as printed wiring boards "PWBs" to obtain improved thermal and dimensional performance properties are known. An example of such can be found in U.S. Patent No. 5,654,081, titled *Integrated Circuit Assembly with Polymeric Underfill Body*, which discusses the use of particular underfill compositions in mounting flip-chip
10 IC devices to circuit boards.

 Underfill compositions can be positioned between the IC and the surface (hereinafter PWB for simplicity) to which it is to be mounted either before or after electrical/metallurgical connections between the IC and PWB are made. If it is to be done after electrical connections are formed, an underfill material can be injected from
15 the sides of gap between the IC and PWB, or through a hole in the PWB located beneath the IC. However, such injection methods tend to be problematic in regard to the time required to inject the underfill, and the difficulty in assuring a complete, uniform distribution of underfill material.

 If it is to be accomplished prior to formation of the electrical connections, the
20 underfill can either be "built-up" on (i.e. printed onto) either the IC or PWB, or provided as a pre-form which is sandwiched between the IC and PWB. Patents referencing the build up process include both U.S. Patent No. 5,654,081 previously discussed and U.S. Patent No. 5,936,847 titled *Low Profile Electronic Circuit Modules*. Printing material onto the IC or the PWB is not always desirable as it tends to overly complicate the
25 handling process and cannot be done in parallel with formation of the ICs and PWBs.

 A patent which utilizes a conductorless pre-form is U.S. Patent No. 6,040,630 titled *Integrated Circuit Package for Flip Chip with Alignment Preform Feature and Method of Forming Same*. Unfortunately, conductorless preforms require the use of pads or other conductors on the IC and/or PWB which can extend through the preform.

A pre-form comprising a filled perforated dielectric structure wherein the dielectric comprises a coated polyimide film and the fill material comprises a transient liquid phase sintered material is utilized in U.S. Patent No. 5,948,533 titled *Vertically Interconnected Electronic Assemblies and Compositions Useful Therefor*. However, the use of coated polyimide films is not desirable in all circumstances.

Thus, there is a need for improved methods and devices for underfilling an IC mounted to a supporting surface such as a PWB.

Summary of the Invention

The present invention is directed to methods and apparatus in which an assembly comprising a thermosetting layer pierced by a plurality of conductors is formed on a release sheet and subsequently sandwiched between an IC and a PWB or other supporting surface and subsequently cured. The release sheet is removed either before or during curing of the thermosetting material. Removal prior to curing may be accomplished via peeling. Removal during curing may be by destruction of the layer by the curing process.

Various objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of preferred embodiments of the invention, along with the accompanying drawings in which like numerals represent like components.

Brief Description of The Drawings

Fig. 1 is a perspective top view of a compliant pre-form interconnect embodying the invention.

Fig. 2 is a cutaway view of a compliant pre-form interconnect embodying the invention.

Fig. 3 is a cutaway view of the interconnect of a compliant pre-form interconnect embodying the invention coupling an integrated circuit to a printed wiring board.

Detailed Description

In Figure 1-3, a preferred pre-form assembly 10 comprises a base layer assembly 100, a sacrificial layer assembly 200, and through conductors 300.

Base layer assembly preferably 100 comprises a single B-staged thermosetting material. Although a thermoplastic material may be used, it is contemplated that a thermosetting material provides additional strength and stability. Preferred B-staged thermosetting materials include but are not necessarily limited to cyanate esters, cycloaliphatic epoxies, bismaleimides, cyanate ester/epoxy copolymers, cyanate ester/bismaleimide copolymers or blends and cycloaliphatic epoxy/bismaleimide copolymers or blends. Although preferably formed from a single layer, it is contemplated that base layer assembly 100 may be a multi-layer assembly.

Sacrificial assembly 200 comprises sacrificial layer 210 and release coating 220. Sacrificial layer 210 is preferably formed from a relatively cheap material such as a polyester or a celluloid film. Release coating 220 preferably is located between the sacrificial layer 210 and base layer assembly 100, and comprises standard silicon, Teflon® or graphite release agents such as commercially available materials which are available from Chemlease™ and Buehler™. An example of such a commercially available material is POL-ESE 233™. In other embodiments, the sacrificial layer assembly 200 may not include release coating 220, particularly if using materials with low natural surface energy and low adhesion to other materials, such as Teflon® and oriented polyimide. In a less-preferred embodiment, the sacrificial layer is not removed but becomes part of the final structure. It is contemplated that in many embodiments, traces of the release coating 220 will remain after removal of sacrificial layer 100.

The use of release coating 220 in conjunction with a cheap sacrificial layer 210 which comprises a polyester or celluloid film is anticipated to provide numerous advantages over any existing protective covering methods and devices such as lowering the cost of sacrificial assembly 200, making it easier to utilize assembly 10, and increasing the flexibility of assembly 10.

Through conductors 300 may be formed by, among other methods, stitching/piercing wire through base layer assembly 100 or forming conductive vias in base layer assembly 100. Through conductors 300 may or may not punch through the sacrificial layer assembly 200 with the choice of whether to have the conductors 300 punch through being at least partially dependent on the method of manufacturing used and the type of object (i.e. a pad, a solder ball, a stud, or some other type) the through connector will ultimately be electrically coupled to. Thus, wire piercing may be the choice for use to connect to a pad or via on a package or board, but a via may be a better choice if connecting to a stud or ball. It is preferred that the choice of type of through conductor and whether it penetrates the sacrificial layer assembly 200 be made so as to accommodate a variety of configurations and manufacturing methods. Figure 2 provides examples of both vias (301 and 302) and wires (303) and examples of a through conductor piercing the entire interconnect (301), piercing the base layer assembly 100 and release coating 220 (302), and piercing only the base layer 100 (303).

If conductive vias are used, it is contemplated that such vias will comprise a solder paste rather than a transient liquid phase sintered material. Preferred solder pastes include PbSn, PbSnAg, Indium alloys, and Au eutectic/alloys, if wire piercing/thermosonic ball formation is used..

It is contemplated that extending the through conductors 300 into the sacrificial layer assembly 200 may provide additional mechanical stability for a corresponding alignment stability.

A preferred method of forming pre-form assembly 10 comprises: providing sacrificial layer 210, coating sacrificial later 210 with release coating 220, applying a thermosetting material 100 on top of release coating 220; curing the thermosetting material 100 to form a B-stage layer; inserting through conductors 300 into thermosetting material 100. Insertion of through conductors 300 preferably comprises either piercing wires 300 into the thermosetting material, or lasing or drilling and subsequently filling holes in thermosetting material 100. The lased vias may be processed by "off-set" lasing to provide a larger bottom diameter footprint , to lessen registration to contact point difficulty . A preferred method of using pre-form assembly 10 comprises: providing an

IC; providing a supporting surface to which the IC is to be mechanically and electrically bonded; providing pre-form assembly 10; applying pre-form assembly 10 to either the IC or supporting surface; peeling away sacrificial layer 210; sandwiching pre-form assembly 10 between the IC and the supporting surface; and curing the base layer assembly of pre-
5 form assembly 10.

A mechanical support structure may be included during the construction of the thermosetting layer 100. In one embodiment thermosetting layer 100 includes a fiber mesh material which consists of but is not limited to glass, graphite, KEVLAR[®], TEFLON[®], or polyester into which the thermoset of layer 100 is impregnated. For
10 additional mechanical support the thermoset may also be formulated with particulate fillers. Such fillers include but are not limited to: alumina, silica, graphite fibers, graphite particles, silicon nitride, silicon carbide, aluminum nitride, diamond, beryllium, and conductive polymer filler.

If a thermal enhancement is required, the preform may include construction using
15 a thermally conductive material. The preferred embodiment would use a non-electrically conductive filler into the thermosetting material 100. Such fillers include but are not limited to silicon nitride, silicon carbide, aluminum nitride, boron nitride, diamond, conductive polymer filler, graphite and alumina. In another embodiment a thermally conductive mesh material may be used in conjunction with the construction of the
20 thermoset layer 100. In this example, a thermally conductive graphite mesh would be impregnated with the thermoset material and become part of layer 100. The thermoset material may or may not include formulation with the conductive filler. In a less preferred embodiment a physical thermal layer 102 would be added to the construction of the preform. For example a copper plane or a phase change film 102 could be added as a
25 center layer between thermoset layers 101 and 103. The thermoset material used may or may not include formulation with the conductive filler, dependent upon the thermal construction desired.

Thus, specific embodiments and applications of compliant preform interconnects have been disclosed. It should be apparent, however, to those skilled in the art that many
30 more modifications besides those already described are possible without departing from

- the inventive concepts herein. The inventive subject matter, therefore, is not to be restricted except in the spirit of the appended claims. Moreover, in interpreting both the specification and the claims, all terms should be interpreted in the broadest possible manner consistent with the context. In particular, the terms “comprises” and
- 5 “comprising” should be interpreted as referring to elements, components, or steps in a non-exclusive manner, indicating that the referenced elements, components, or steps may be present, or utilized, or combined with other elements, components, or steps that are not expressly referenced.

CLAIMS

What is claimed is:

1. An IC assembly comprising:
an IC;
a supporting surface; and
an interconnect mechanically and electrically coupling the IC to the supporting surface, the interconnect comprising a plurality of through conductors electrically bonded to the IC and the supporting surface, and a dielectric base layer mechanically bonded to the through conductors, IC and supporting surface, and traces of a release coating positioned between the dielectric base layer and either the IC or the supporting surface, the release coating traces comprising a residue of a composition which differed from the composition of the IC, supporting surface, and dielectric base layer.
2. The IC assembly of claim 1 wherein the IC dielectric base layer comprises a material from at least one of the following groups: cyanate esters; cycloaliphatic epoxies; bismaleimides; cyanate ester and epoxy copolymers; cyanate ester and bismaleimide copolymers or blends; and cycloaliphatic epoxy and bismaleimide copolymers or blends.
3. The IC assembly of claim 2 wherein the traces of a release coating at least partially comprise residues of silicon, Teflon[®], or graphite release agents.
4. The IC assembly of claim 3 wherein the through conductors comprise wires.
5. The IC assembly of claim 4 wherein the through conductors comprise solder paste vias, the solder paste comprising at least one of the following: PbSn, PbSnAg, an Indium alloy, and an Au eutectic alloy.
6. The IC assembly of claim 1 wherein the dielectric base layer comprises a fiber mesh material impregnated with a thermoset or a thermoset intermixed with a particulate filler.

7. The IC assembly of claim 6 wherein the dielectric base layer comprises the fiber mesh material impregnated with a thermoset, and the fiber mesh material comprises at least one of the following: glass, graphite, KEVLAR[®], TEFLON[®], and polyester.
8. The IC assembly of claim 6 wherein the dielectric base layer comprises the fiber mesh material impregnated with a thermoset, and the fiber mesh material is thermally conductive.
9. The IC assembly of claim 6 wherein the dielectric base layer comprises the thermoset intermixed with a particulate filler, and the filler comprises at least one of: alumina, silica, graphite fibers, graphite particles, silicon nitride, silicon carbide, aluminum nitride, diamond, beryllium, and conductive polymer filler.
10. The IC assembly of claim 6 wherein the dielectric base layer comprises the thermoset intermixed with a thermally conductive, non-electrically conductive particulate filler. and the filler comprises at least one of: silicon nitride, silicon carbide, aluminum nitride, boron nitride, diamond, conductive polymer filler, graphite and alumina.
11. The IC assembly of claim 6 wherein the dielectric base layer comprises a physical thermal layer sandwiched between two thermoset layers.
12. The IC assembly of claim 11 wherein the thermal layer comprises copper or a phase change film.
13. A method for coupling an IC to a supporting surface comprising:
providing an IC;
providing a supporting surface to which the IC is to be mechanically and electrically bonded;
providing a pre-form assembly comprising a base layer and a sacrificial layer;
applying the pre-form assembly to either the IC or supporting surface;
peeling away the sacrificial layer;

sandwiching the peeled pre-form assembly between the IC and the supporting surface; and

curing the base layer.

14. The method of claim 13 wherein providing the preform assembly comprises:
providing a sacrificial layer;
coating the sacrificial later with a release coating;
applying a thermosetting material on top of the release coating;
curing the thermosetting material to form a B-stage layer; and
inserting through conductors into the thermosetting material.
15. The method of claim 14 wherein the step of inserting through conductors into the thermosetting material comprises either piercing wires into the thermosetting material, or lasing or drilling and subsequently filling holes in the thermosetting material with a solder paste.
16. The method of claim 13 wherein the base layer comprises a fine mesh fiber material impregnated with a thermoset.
17. The method of claim 16 wherein the fine mesh fiber is thermally conductive.
18. The method of claim 16 wherein the fine mesh fiber is electrically non-conductive.
19. The method of claim 13 wherein the base layer comprises a thermoset intermixed with a particle filler.
20. The method of claim 19 wherein the particle filler is thermally conductive.
21. The method of claim 19 wherein the particle filler is electrically non-conductive.