# METHODS OF SELECTIVELY BUMPING INTEGRATED CIRCUIT SUBSTRATES AND RELATED STRUCTURES

## RELATED APPLICATION

This application claims the benefit of priority from U.S. Provisional Patent Application No. 60/448,096 filed on February 18, 2003, the disclosure of which is hereby incorporated herein by reference in its entirety.

## FIELD OF THE INVENTION

The present invention relates to the field of integrated circuits and more particularly to methods of bumping integrated circuit substrates.

## BACKGROUND OF THE INVENTION

High performance microelectronic devices often use solder balls or solder bumps for electrical interconnection to other microelectronic devices. For example, a very large scale integration (VLSI) chip may be electrically connected to a circuit board or other next level packaging substrate using solder balls or solder bumps. This connection technology is also referred to as "Controlled Collapse Chip Connection--C4" or "flip-chip" technology, and will be referred to herein as solder bumps.

According to solder bump technology developed by IBM, solder bumps are formed by evaporation through openings in a shadow mask which is clamped to an integrated circuit wafer. For example, U.S. Pat. No. 5,234,149 entitled "Debondable Metallic Bonding Method" to Katz et al. discloses an electronic device with chip wiring terminals and metallization layers. The wiring terminals are typically essentially aluminum, and the metallization layers may include a titanium or chromium localized adhesive layer, a co-deposited localized chromium copper layer, a localized wettable copper layer, and a localized gold or tin capping layer. An evaporated localized lead-tin solder layer is located on the capping layer.

Solder bump technology based on an electroplating method has also been actively pursued. The electroplating method is particularly useful for

larger substrates and smaller bumps. In this method, an "under bump metallurgy" (UBM) layer is deposited on a microelectronic substrate having contact pads thereon, typically by evaporation or sputtering. A continuous under bump metallurgy layer is typically provided on the pads and on the substrate between the pads to allow current flow during solder plating.

An example of an electroplating method with an under bump metallurgy layer is discussed in U.S. Pat. No. 5,162,257 entitled "Solder Bump Fabrication Method" to Yung and assigned to the assignee of the present application. In this patent, the under bump metallurgy layer includes a chromium layer adjacent the substrate and pads, a top copper layer which acts as a solderable metal, and a phased chromium/copper layer between the chromium and copper layers. The base of the solder bump is preserved by converting the under bump metallurgy layer between the solder bump and contact pad into an intermetallic of the solder and the solderable component of the under bump metallurgy layer.

## SUMMARY OF THE INVENTION

According to embodiments of the present invention, an integrated circuit substrate includes a metal layer thereon, a barrier layer is formed on the integrated circuit substrate including the metal layer, and a conductive bump is formed on the barrier layer. More particularly, the barrier layer is between the conductive bump and the substrate, and the conductive bump is offset from the metal layer. After forming the conductive bump, at least portions of the barrier layer are removed from the metal layer thereby exposing the metal layer while a portion of the barrier layer is maintained between the conductive bump and the substrate. The metal layer may be an aluminum layer, and/or the barrier layer may be a layer of TiW. Moreover, the metal layer, the barrier layer, and the conductive bump may be layers of different materials.

A conductive under bump metallurgy layer may also be formed on the barrier layer before forming the conductive bump. Before removing the barrier layer, the conductive under bump metallurgy layer may be removed from the barrier layer opposite the metal layer while maintaining a portion of the

conductive under bump metallurgy layer between the conductive bump and the substrate. The conductive under bump metallurgy layer may include a layer of copper, and the conductive under bump metallurgy layer and the barrier layer may be layers of different materials.

A second barrier layer may also be formed on the under bump metallurgy layer before forming the conductive bump with the second barrier layer and the under bump metallurgy layer being layers of different materials. Moreover, the second barrier layer may be between the conductive bump and the conductive under bump metallurgy layer. The second barrier layer may be a layer of nickel, and the under bump metallurgy layer may be a layer of copper.

The second barrier layer may be selectively formed on a portion of the under bump metallurgy layer with the second barrier layer being offset from the metal layer. Moreover, the conductive bump may be selectively formed on the second barrier layer offset from the metal layer. In addition, the second barrier layer and the conductive bump may be selectively formed using a same mask. The conductive bump may be at least one of a solder bump, a gold bump, and/or a copper bump. Moreover, the conductive bump may be selectively plated on the barrier layer offset from the metal layer.

The integrated circuit substrate may also include an input/output pad thereon. The barrier layer may be formed on the substrate including the metal layer and the input/output pad, and the conductive bump may be formed on the barrier layer opposite the input/output pad. More particularly, the metal layer and the bump pad may both be layers of aluminum.

The integrated circuit substrate may include an input/output pad thereon, the barrier layer may be formed on the substrate including the metal layer and the input/output pad, and the conductive bump may be electrically coupled to the input/output pad after removing the barrier layer from the metal layer. Moreover, the metal layer and the input/output pad may both be layers of aluminum. In addition, the conductive bump may be formed on the barrier layer opposite the input/output pad, or the conductive bump may be offset from the input/output pad. A second substrate may also be bonded to the conductive bump after removing the barrier layer from the metal layer.

According to additional embodiments of the present invention, methods of bumping an integrated circuit device include forming a barrier layer on an integrated circuit substrate wherein the barrier layer is offset from an exposed metal layer on the integrated circuit substrate. A conductive bump is formed on the barrier layer with the barrier layer being between the conductive bump and the substrate. Moreover, the conductive bump is offset from the metal layer, and the barrier layer, the conductive bump, and the metal layer may be layers of different conductive materials.

The barrier layer may be a layer of titanium tungsten, and the exposed metal layer may be a layer of aluminum. In addition, the conductive bump may be at least one of a solder bump, a gold bump, and/or a copper bump. A conductive under bump metallurgy layer may also be provided between the barrier layer and the conductive bump, and a second substrate may be bonded to the conductive bump.

The integrated circuit substrate may also include an input/output pad on the integrated circuit substrate wherein the barrier layer and the conductive bump are electrically connected to the input/output pad. Moreover, the input/output pad and the metal layer may each be layers of aluminum. In addition, the conductive bump may be on the barrier layer opposite the input/output pad, and the conductive bump may be offset from the input/output pad. An under bump metallurgy layer may also be between the barrier layer and the conductive bump, and the under bump metallurgy layer and the barrier layer may be layers of different materials.

According to still additional embodiments of the present invention, an integrated circuit device includes an integrated circuit substrate having an exposed metal layer thereon. A barrier layer is on the integrated circuit substrate offset from the exposed metal layer, and a conductive bump is on the barrier layer. More particularly, the barrier layer is between the conductive bump and the substrate, the conductive bump is offset from the metal layer, and the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-4 are cross sectional views illustrating integrated circuit devices during intermediate fabrication steps according to first embodiments of the present invention.

Figures 5-8 are cross sectional views illustrating integrated circuit devices during intermediate fabrication steps according to second embodiments of the present invention.

Figures 9-12 are cross sectional views illustrating integrated circuit devices during intermediate fabrication steps according to third embodiments of the present invention.

Figures 13-14 are cross sectional views illustrating integrated circuit devices during intermediate fabrication steps according to fourth embodiments of the present invention.

Figures 15-17 are perspective views illustrating assembly of electronic devices according to embodiments of the present invention.

## DETAILED DESCRIPTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, thicknesses of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout.

It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element, or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Also, when an element is referred to as being "bonded" to another element, it can be directly bonded to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly bonded" to another element, there are

no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. Finally, the term "directly" means that there are no intervening elements.

According to embodiments of the present invention, methods may be provided that allow bumping of integrated circuit substrates (such as integrated circuit wafers) while providing metal layers (such as exposed aluminum layers) exposed on the substrate. A metal layer, such as an aluminum layer, may be used to provide a wirebond contact, an exposed Input/output pad, a fuse and/or a reflector. Moreover, a conductive bump, such as a solder bump may be provided on the substrate to provide electrical and/or mechanical interconnection with another substrate. By providing an exposed metal layer after forming bumps on the substrate, a metal layer input/out pad can provide a wirebond pad after forming bumps, and/or a metal layer laser fuse can be opened using a laser after forming bumps.

First embodiments of the present invention are discussed below with reference to Figures 1-4. As shown in Figure 1, an integrated circuit substrate **21** may have a metal layer **23** and a passivation layer **25** thereon. The integrated circuit substrate **21** may include a semiconductor substrate (such as a silicon, gallium arsenide, gallium nitride, and/or silicon carbide substrate) having electronic devices (such as transistors, diodes, resistors, capacitors, and/or inductors) formed thereon. As used herein, the term substrate may be used to refer to a wafer including a plurality of integrated circuit devices thereon or to an integrated circuit die including a single integrated circuit device thereon. Typically, a plurality of die can be cut from a single wafer after fabrication of a plurality of integrated circuit devices on the single wafer. In other alternatives, the term substrate may be used to refer to another layer of packaging substrate such as a printed circuit board.

The metal layer **23**, for example, may provide an input/output pad for electronic devices of the substrate **21** to be used as an input/output pad for subsequent wire bonding. In an alternative, the metal layer **23** may provide a fuse that can be cut mechanically and/or with a laser to provide coupling/decoupling of redundant circuitry on the substrate **21**. In another

alternative, the metal layer **23** may provide a pad for electrical probing of circuitry on the substrate **21**.

The passivation layer **25** may include an inorganic material (such as silicon dioxide and/or silicon nitride) and/or an organic material (such as polyimide). As shown, a hole in the passivation layer **25** may expose portions of the metal layer **23**. More particularly, the passivation layer **25** may be formed over the metal layer **23**, and then portions of the passivation layer **25** may be selectively removed to expose portions of the metal layer **23**. By providing that portions of the metal layer **23** are exposed, the metal layer may be subsequently probed, cut, and/or used as a wire bonding pad.

As shown in Figure 2, a first barrier layer **27** (such as a layer of TiW, TiN, and/or combinations thereof) may be formed on the passivation layer **25** and the exposed portions of the metal layer **23**, for example, using sputtering, evaporation, and/or chemical vapor deposition (CVD). The exposed surface of the first barrier layer **27** may be subjected to cleaning using wet and/or dry cleaning operations before a subsequent step of forming under bump metallurgy layer **29**. The first barrier layer **27** may be selected to provide adhesion between the under bump metallurgy layer **29** and the passivation layer **25**; to provide electrical conduction of signals between under bump metallurgy layer **29** and the substrate **21**; and/or to provide an etch selectivity with respect to the metal layer **23**. Accordingly, the first barrier layer **27** may be removed from the metal layer **23** without significantly damaging the metal layer **23**.

The conductive under bump metallurgy layer **29** may then be formed on the barrier layer **27** opposite the substrate **21** and the metal layer **23**. More particularly, the conductive under bump metallurgy layer **29** may include copper (Cu). A mask layer **31** (such as a layer of photoresist and/or polymer) may be formed on the conductive under bump metallurgy layer **29**, and a hole **33** may be formed in the mask layer **31** to provide a plating template. More particularly, the mask layer **31** may be a layer of photoresist that has been selectively exposed and developed using photolithographic techniques to form the hole **33**.

A second barrier layer **32** (such as a layer of nickel) and a bumping material **35** (such as a tin based solder, gold, and/or copper) may then be

selectively formed on portions of the conductive under bump metallurgy layer **29** exposed by the hole **33**. For example, the second barrier layer **32** and the bumping material **35** may be electroplated with the under bump metallurgy layer **29** providing a plating electrode and a current path under the mask **31**. In an alternative, electroless plating may be used so that a current path under the mask is not needed during plating. Other deposition techniques may also be used. After forming the second barrier layer **32** and the bumping material **35**, the mask **31** can be stripped, for example, using a dry and/or wet process chemistry.

As shown in Figure 3, portions of the conductive under bump metallurgy layer **29** not covered by the bumping material **35** and/or the second barrier layer **32** can be removed. More particularly, portions of the conductive under bump metallurgy layer **29** can be removed using an etch chemistry that removes the conductive under bump metallurgy layer **29** preferentially with respect to the first barrier layer **27**. Accordingly, the first barrier layer **27** may protect the metal layer **23** while removing portions of the under bump metallurgy layer **29**. With a conductive under bump metallurgy layer **29** of copper (Cu) and a first barrier layer **27** of titanium-tungsten (TiW), Ammonium Hydroxide may be used to selectively remove the conductive under bump metallurgy layer **29** while maintaining the metal layer **23**.

Portions of the first barrier layer **27** not covered by the bumping material **35**, the second barrier layer **32**, and/or remaining portions of the under bump metallurgy layer **29** can then be removed using an etch chemistry that removes the first barrier layer **27** preferentially with respect to the metal layer **23**. Accordingly, the first barrier layer **27** may be removed without significantly damaging the metal layer **23**. With a first barrier layer **27** of titanium-tungsten (TiW) and a metal layer **23** of aluminum (Al), portions of the first barrier layer **27** may be removed using a mixture including:

Hydrogen peroxide - 10-20%;
Sulfosalicylic acid - 2-30 grams/liter;
Potassium sulfate - 25-200 grams/liter;
Benzotrizole - 1-10 grams/liter;
Water for makeup;
Temp: 30 to 70 degC; and
pH<7.

The structure of Figure 3 can then be heated so that the bumping material **35** forms a ball while the metal layer **23** (such as an aluminum layer) is exposed as shown in Figure 4. With a tin based solder bumping material, for example, the bumping material **35** may be fluxed, reflowed, and cleaned to provide the ball of bumping material **35** of Figure 4. With a gold bumping material, the bumping material **35** may be annealed. In an alternative, portions of the under bump metallurgy layer **29** and the barrier layer **27** can be removed after heating the bumping material to form a ball. In another alternative, the bumping material **35** may be bonded to a compatible substrate without first forming a ball.

While not shown in Figure 4, bumping material **35**, the second barrier layer **32**, the remaining portion of the conductive under bump metallurgy layer **29**, and the remaining portion of the first barrier layer **27** may be electrically coupled to the substrate through a hole in the passivation layer **25** and/or a redistribution routing conductor. The bumping material **35** can be electrically coupled to a remote contact pad using a redistribution routing conductor as discussed, for example, in U.S. Patent No. 5,892,179, U.S. Patent No. 6,329,608, and/or U.S. Patent No. 6,389,691. The disclosures of each of these patents are hereby incorporated herein in their entirety by reference.

Accordingly, the bumping material **35** can be used to provide electrical and/or mechanical coupling to another substrate (such as another integrated circuit semiconductor device and/or a printed circuit board) while the metal layer **23** is exposed. Accordingly, the metal layer **23** may be burned, cut, probed, and/or wire bonded after forming the bumping material **35** and/or after bonding the bumping material **35** to another substrate.

Second embodiments of the present invention are discussed below with reference to Figures 5-8. As shown in Figure 5, an integrated circuit substrate **121** may have a metal layer **123** and an interconnection layer **119** thereon, and a passivation layer **125** may be provided on the metal layer **123**, the interconnection layer **119**, and the substrate **121**. The metal layer **123** and the interconnection layer **119** may be patterned from a same metal layer (such as a same aluminum layer). The integrated circuit substrate **121** may include a semiconductor substrate (such as a silicon, gallium arsenide, gallium nitride, and/or silicon carbide substrate) having electronic devices

(such as transistors, diodes, resistors, capacitors, and/or inductors) formed thereon. As used herein, the term substrate may be used to refer to a wafer including a plurality of integrated circuit devices thereon or to an integrated circuit die including a single integrated circuit device thereon. Typically, a plurality of die can be cut from a single wafer after fabrication of a plurality of integrated circuit devices on the single wafer. In other alternatives, the term substrate may be used to refer to another layer of packaging substrate such as a printed circuit board.

The metal layer **123**, for example, may provide an input/output pad for electronic devices of the substrate **121** to be used as an input/output pad for subsequent wire bonding. In an alternative, the metal layer **123** may provide a fuse that can be cut mechanically and/or with a laser to provide coupling/decoupling of redundant circuitry on the substrate **121**. In another alternative, the metal layer **123** may provide a pad for electrical probing of circuitry on the substrate **121**. The interconnection layer **119** may provide electrical and mechanical interconnection through a bumping material to a next level substrate (such as a printed circuit board or an integrated circuit device) as discussed in greater detail below. The metal layer **123** and the interconnection layer **119** may both include aluminum.

The passivation layer **125** may include an inorganic material (such as silicon dioxide and/or silicon nitride) and/or an organic material (such as polyimide). As shown, holes in the passivation layer **125** may expose portions of the metal layer **123** and portions of the interconnection layer **119**. More particularly, the passivation layer **125** may be formed over the metal layer **123** and the interconnection layer **119**, and then portions of the passivation layer **125** may be selectively removed to expose portions of the metal layer **123** and the interconnection layer **119**. By providing that portions of the metal layer **123** are exposed, the metal layer may be subsequently probed, cut, and/or used as a wire bonding pad.

As shown in Figure 6, a first barrier layer **127** (such as a layer of TiW, TiN, and/or combinations thereof) may be formed on the passivation layer **125**, on the exposed portions of the metal layer **123**, and on the exposed portions of the interconnection layer **119**, for example, using sputtering, evaporation, and/or chemical vapor deposition (CVD). The exposed surface

of the first barrier layer **127** may be subjected to cleaning using wet and/or dry cleaning operations before a subsequent step of forming under bump metallurgy layer **129**. The first barrier layer **127** may be selected to provide adhesion between the under bump metallurgy layer **129** and the passivation layer **125**; to provide adhesion between the under bump metallurgy layer **129** and the interconnection layer **119**; to provide electrical conduction of signals between under bump metallurgy layer **129** and the substrate **121**; and/or to provide an etch selectivity with respect to the metal layer **123**. Accordingly, the first barrier layer **127** may be removed from the metal layer **123** without significantly damaging the metal layer **123**.

The conductive under bump metallurgy layer **129** may then be formed on the barrier layer **127** opposite the substrate **121**, the metal layer **123**, and the interconnection layer **119**. More particularly, the conductive under bump metallurgy layer **129** may include copper (Cu). A mask layer **131** (such as a layer of photoresist and/or polymer) may be formed on the conductive under bump metallurgy layer **129**, and a hole **133** may be formed in the mask layer **131** to provide a plating template exposing portions of the under bump metallurgy layer **129** opposite the interconnection layer **119**. More particularly, the mask layer **131** may be a layer of photoresist that has been selectively exposed and developed using photolithographic techniques to form the hole **133**.

A second barrier layer **132** (such as a layer of nickel) and a bumping material **135** (such as a tin based solder, gold, and/or copper) may then be selectively formed on portions of the conductive under bump metallurgy layer **129** exposed by the hole **133**. For example, the second barrier layer **132** and the bumping material **135** may be electroplated with the under bump metallurgy layer **129** providing a plating electrode and a current path under the mask **131**. In an alternative, electroless plating may be used so that a current path under the mask is not needed during plating. Other deposition techniques may also be used. After forming the second barrier layer **132** and the bumping material **135**, the mask **131** can be stripped, for example, using a dry and/or wet process chemistry.

As shown in Figure 7, portions of the conductive under bump metallurgy layer **129** not covered by the bumping material **135** and/or the

second barrier layer **132** can be removed. More particularly, portions of the conductive under bump metallurgy layer **129** can be removed using an etch chemistry that removes the conductive under bump metallurgy layer **129** preferentially with respect to the first barrier layer **127**. Accordingly, the first barrier layer **127** may protect the metal layer **123** while removing portions of the under bump metallurgy layer **129**. With a conductive under bump metallurgy layer **129** of copper (Cu) and a first barrier layer **127** of titanium-tungsten (TiW), Ammonium Hydroxide may be used to selectively remove the conductive under bump metallurgy layer **129** while maintaining the metal layer **123**.

Portions of the first barrier layer **127** not covered by the bumping material **135**, the second barrier layer **132**, and/or remaining portions of the under bump metallurgy layer **129** can then be removed using an etch chemistry that removes the first barrier layer **127** preferentially with respect to the metal layer **123**. Accordingly, the first barrier layer **127** may be removed without significantly damaging the metal layer 123. With a first barrier layer 127 of titanium-tungsten (TiW) and a metal layer 123 of aluminum (Al), portions of the first barrier layer 127 may be removed using a mixture including:

Hydrogen peroxide - 10-20%;
Sulfosalicylic acid - 2-30 grams/liter;
Potassium sulfate - 25-200 grams/liter;
Benzotrizole - 1-10 grams/liter;
Water for makeup;
Temp: 30 to 70 degC; and
pH<7.

The structure of Figure 7 can then be heated so that the bumping material **135** forms a ball while the metal layer **123** (such as an aluminum layer) is exposed as shown in Figure 8. With a tin based solder bumping material, for example, the bumping material **135** may be fluxed, reflowed, and cleaned to provide the ball of bumping material **135** of Figure 8. With a gold bumping material, the bumping material **135** may be annealed. In an alternative, portions of the under bump metallurgy layer **129** and the barrier layer **127** can be removed after heating the bump material to form a ball. In

another alternative, the bumping material **135** may be bonded to a compatible substrate without first forming a ball.

While not shown in Figure 8, bumping material **135**, the second barrier layer **132**, the remaining portion of the conductive under bump metallurgy layer **129**, and the remaining portion of the first barrier layer **127** may be electrically coupled to the interconnection layer **119** through a redistribution routing conductor so that the bumping material **135** is offset from the interconnection layer **119**.

Accordingly, the bumping material **135** can be used to provide electrical and/or mechanical coupling to another substrate (such as another integrated circuit semiconductor device and/or a printed circuit board) while the metal layer **123** is exposed. Accordingly, the metal layer **123** may be burned, cut, probed, and/or wire bonded after forming the bumping material **135** and/or after bonding the bumping material **135** to another substrate.

Third embodiments of the present invention are discussed below with reference to Figures 9-12. As shown in Figure 9, an integrated circuit substrate 321 may have a metal layer 323 and an interconnection layer 319, and a passivation layer 325 may be provided on the metal layer 323, the interconnection layer **319**, and the substrate **321**. The metal layer **323** and the interconnection layer 319 may be patterned from a same metal layer (such as a same aluminum layer). The integrated circuit substrate 321 may include a semiconductor substrate (such as a silicon, gallium arsenide, gallium nitride, and/or silicon carbide substrate) having electronic devices (such as transistors, diodes, resistors, capacitors, and/or inductors) formed thereon. As used herein, the term substrate may be used to refer to a wafer including a plurality of integrated circuit devices thereon or to an integrated circuit die including a single integrated circuit device thereon. Typically, a plurality of die can be cut from a single wafer after fabrication of a plurality of integrated circuit devices on the single wafer. In other alternatives, the term substrate may be used to refer to another layer of packaging substrate such as a printed circuit board.

The metal layer **323**, for example, may provide an input/output pad for electronic devices of the substrate **321** to be used as an input/output pad for subsequent wire bonding. In an alternative, the metal layer **323** may provide

a fuse that can be cut mechanically and/or with a laser to provide coupling/decoupling of redundant circuitry on the substrate **321**. In another alternative, the metal layer **323** may provide a pad for electrical probing of circuitry on the substrate **321**. The interconnection layer **219** may provide electrical and mechanical interconnection through a bumping material to a next level substrate (such as a printed circuit board or an integrated circuit device) as discussed in greater detail below. The metal layer **323** and the interconnection layer **319** may both include aluminum.

The passivation layer **325** may include an inorganic material (such as silicon dioxide and/or silicon nitride) and/or an organic material (such as polyimide). As shown, holes in the passivation layer **325** may expose portions of the metal layer **323** and portions of the interconnection layer **319**. More particularly, the passivation layer **325** may be formed over the metal layer **323** and the interconnection layer **319**, and then portions of the passivation layer **325** may be selectively removed to expose portions of the metal layer **323** and the interconnection layer **319**. By providing that portions of the metal layer **323** are exposed, the metal layer may be subsequently probed, cut, and/or used as a wire bonding pad.

As shown in Figure 10, a first barrier layer **327** (such as a layer of TiW, TiN, and/or combinations thereof) may be formed on the passivation layer **325**, on the exposed portions of the metal layer **323**, and on the exposed portions of the interconnection layer **319**, for example, using sputtering, evaporation, and/or chemical vapor deposition (CVD). The exposed surface of the first barrier layer **327** may be subjected to cleaning using wet and/or dry cleaning operations before a subsequent step of forming under bump metallurgy layer **329**. The first barrier layer **327** may be selected to provide adhesion between the under bump metallurgy layer **329** and the passivation layer **325**; to provide adhesion between the under bump metallurgy layer **329** and the interconnection layer **319**; to provide electrical conduction of signals between under bump metallurgy layer **329** and the substrate **321**; and/or to provide an etch selectivity with respect to the metal layer **323**. Accordingly, the first barrier layer **327** may be removed from the metal layer **323** without significantly damaging the metal layer **323**.

The conductive under bump metallurgy layer **329** may then be formed on the barrier layer **327** opposite the substrate **321**, on the metal layer **323**, and on the interconnection layer **319**. More particularly, the conductive under bump metallurgy layer **329** may include copper (Cu). In addition, a dam layer **330** may be formed on the under bump metallurgy layer **329** opposite the substrate. The dam layer **330** may be formed of a material such as chromium to which a subsequently formed bump material does not wet during reflow.

A mask layer **331** (such as a layer of photoresist and/or polymer) may be formed on the conductive under bump metallurgy layer **329**, and a hole **333** may be formed in the mask layer **331** to provide a plating template exposing portions of the under bump metallurgy layer **329** opposite the interconnection layer **319**. The mask layer **331** may be a layer of photoresist that has been selectively exposed and developed using photolithographic techniques to form the hole **333**. After forming the hole **333**, portions of the dam layer **330** exposed through the hole **333** may be removed to expose portions of the under bump metallurgy layer **329**.

The hole **333** through the mask layer **331** may have an elongate portion and a relatively wide portion when viewed perpendicular from the substrate **321** (i.e. when viewed from above the substrate **321** in the orientation illustrated in figure 10). More particularly, the relatively wide portion of the hole **333** may be offset from the interconnection layer **319**, and the elongate portion of the hole **333** may extend from the relatively wide portion of the hole to adjacent the interconnection layer **319**. For example, the hole **333** may have a keyhole shape with the relatively wide (i.e. circular) portion of the keyhole shape offset from the interconnection layer **319**, and with the elongate portion of the keyhole shape extending adjacent the interconnection layer **319**.

A second barrier layer **332** (such as a layer of nickel) and a bumping material **335** (such as a tin based solder, gold, and/or copper) may then be selectively formed on portions of the conductive under bump metallurgy layer **329** exposed by the hole **333**. For example, the second barrier layer **332** and the bumping material **335** may be electroplated with the under bump metallurgy layer **329** providing a plating electrode and a current path under the mask **331**. In an alternative, electroless plating may be used so that a

current path under the mask is not needed during plating. Other deposition techniques may also be used. After forming the second barrier layer **332** and the bumping material **335**, the mask **331** can be stripped, for example, using a dry and/or wet process chemistry. Accordingly, the second barrier layer **332** and the bumping material **335** may have enlarged width portions spaced apart from the interconnection layer **319** and elongate portions between the enlarged width portions and the interconnection layer **319**. As shown in Figure 11, the mask **331** may be removed.

As shown in Figure 12, the bumping material **335** may be subjected to a reflow operation. Due to differences in radius of curvature over the enlarged width and elongate portions of the bumping material **335**, internal pressures may drive bumping material from the elongate portion to the enlarged width portion. Accordingly, a relatively thin portion **335b** may remain at the elongate portion while a relatively thick portion **335a** may form at the enlarged width portion. Moreover, the dam layer **330** may confine the bumping material **335** to the enlarged width and elongate portions during reflow.

Portions of the conductive under bump metallurgy layer **329** not covered by the bumping material **335** (including relatively thick and thin portions **335a-b**) and/or the second barrier layer **332** can be removed. More particularly, portions of the conductive under bump metallurgy layer **329** can be removed using an etch chemistry that removes the conductive under bump metallurgy layer **329** preferentially with respect to the first barrier layer **327**. Accordingly, the first barrier layer **327** may protect the metal layer **323** while removing portions of the under bump metallurgy layer **329**. With a conductive under bump metallurgy layer **329** of copper (Cu) and a first barrier layer **327** of titanium-tungsten (TiW), Ammonium Hydroxide may be used to selectively remove the conductive under bump metallurgy layer **329** while maintaining the metal layer **323**.

Portions of the first barrier layer **327** not covered by the bumping material **335**, the second barrier layer **332**, and/or remaining portions of the under bump metallurgy layer **329** can then be removed using an etch chemistry that removes the first barrier layer **327** preferentially with respect to the metal layer **323**. Accordingly, the first barrier layer **327** may be removed without significantly damaging the metal layer **323**. With a first barrier layer

**327** of titanium-tungsten (TiW) and a metal layer **323** of aluminum (Al), portions of the first barrier layer **327** may be removed using a mixture including:

Hydrogen peroxide - 10-20%;
Sulfosalicylic acid - 2-30 grams/liter;
Potassium sulfate - 25-200 grams/liter;
Benzotrizole - 1-10 grams/liter;
Water for makeup;
Temp: 30 to 70 degC; and
pH<7.

Redistribution routing conductors are discussed, for example, in U.S. Patent No. 5,892,179, U.S. Patent No. 6,329,608, and/or U.S. Patent No. 6,389,691. The disclosures of each of these patents are hereby incorporated herein in their entirety by reference.

In an alternative, portions of the under bump metallurgy layer **327** and the first barrier layer **329** not covered by the second barrier layer **332** and/or the bumping material **335** of Figure 11 may be removed before reflowing the bumping material **335**. Accordingly, the dam layer **330** may be omitted, and flow of the bumping material **335** may be confined by using a passivation layer **325** to which the bumping material does not wet. After removing portions of under bump metallurgy layer **329** and first barrier layer **327**, the bumping material may be subjected to reflow so that a relatively thin layer **335b** is provided on elongate portions and a relatively thick layer **335a** is provided on enlarged width portions as shown in Figure 12.

With a tin based solder bumping material, for example, the bumping material **335** may be fluxed, reflowed, and cleaned to provide the ball of bumping material **335** of Figure 12. With a gold bumping material, the bumping material **335** may be annealed.

As shown in Figure 12, a ball of the bumping material **335** may be formed, and the ball (relatively thick portion **335b**) of the bumping material **335** may be electrically connected to the interconnection layer **319** through a redistribution routing conductor comprising remaining elongate portions of the first barrier layer **327**, the under bump metallurgy layer **329**, and/or the relatively thin portion **335b** of the bumping material **335**. Moreover, the metal

layer **323** (such as an aluminum layer) may be exposed as shown in Figure 12.

Accordingly, the bumping material **335** can be used to provide electrical and/or mechanical coupling to another substrate (such as another integrated circuit semiconductor device and/or a printed circuit board) while the metal layer **323** is exposed. Accordingly, the metal layer **323** may be burned, cut, probed, and/or wire bonded after forming the bumping material **335** and/or after bonding the bumping material **335** to another substrate.

Fourth embodiments of the present invention are discussed below with reference to Figures 13-14. As shown in Figure 13, an integrated circuit substrate **421** may have first and second metal layers **423a-b** and a first passivation layer **425a** may be provided on the metal layers **423a-b**, and the substrate **421**. The metal layers **423a-b** may be patterned from a same metal layer (such as a same aluminum layer). The integrated circuit substrate **421** may include a semiconductor substrate (such as a silicon, gallium arsenide, gallium nitride, and/or silicon carbide substrate) having electronic devices (such as transistors, diodes, resistors, capacitors, and/or inductors) formed thereon. As used herein, the term substrate may be used to refer to a wafer including a plurality of integrated circuit devices thereon or to an integrated circuit die including a single integrated circuit device thereon. Typically, a plurality of die can be cut from a single wafer after fabrication of a plurality of integrated circuit devices on the single wafer. In other alternatives, the term substrate may be used to refer to another layer of packaging substrate such as a printed circuit board.

The metal layer **423a**, for example, may provide an input/output pad for electronic devices of the substrate **421** to be used as an input/output pad for subsequent wire bonding. In an alternative, the metal layer **423** may provide a fuse that can be cut mechanically and/or with a laser to provide coupling/decoupling of redundant circuitry on the substrate **421**. In another alternative, the metal layer **423** may provide a pad for electrical probing of circuitry on the substrate **421**. The metal layer **423b** may provide an input/output pad for electronic devices of the substrate **421**. The metal layers **423a-b** may both include aluminum.

The first passivation layer **425a** may include an inorganic material (such as silicon dioxide and/or silicon nitride) and/or an organic material (such as polyimide). As shown, holes in the first passivation layer **425a** may expose portions of the metal layers **423a-b**. More particularly, the first passivation layer **425a** may be formed over the metal layers **423a-b**, and then portions of the first passivation layer **425a** may be selectively removed to expose portions of the metal layers **423a-b**. By providing that portions of the metal layer **423a** are exposed, the metal layer **423a** may be subsequently probed, cut, and/or used as a wire bonding pad.

An interconnection layer **419** may then be formed on the first passivation layer **425a** and on portions of the second metal layer **423b**. More particularly, the interconnection layer **419** may extend from exposed portions of the second metal layer **423b** to provide electrical connection with subsequently formed bumping material that is offset from the metal layer **423b**. The metal layers **423a-b** and the interconnection layer **419** may both include aluminum.

In addition, a second passivation layer **425b** may be formed on the interconnection layer **419**, on the first passivation layer **425a**, and on exposed portions of the first metal layer **423a**. Holes may then be formed in the second passivation layer **425b** to expose portions of the interconnection layer **419** and the first metal layer **423a**. The second passivation layer **425b** may include an inorganic material (such as silicon dioxide and/or silicon nitride) and/or an organic material (such as polyimide). The interconnection layer **419** may provide electrical and mechanical interconnection through a bumping material to a next level substrate (such as a printed circuit board or an integrated circuit device) as discussed in greater detail below.

A first barrier layer **427** (such as a layer of TiW, TiN, and/or combinations thereof) may be formed on the second passivation layer **425b**, and on exposed portions of the interconnection layer **419**, the first passivation layer **425a**, and the first metal layer **423a**, for example, using sputtering, evaporation, and/or chemical vapor deposition (CVD). The exposed surface of the first barrier layer **427** may be subjected to cleaning using wet and/or dry cleaning operations before a subsequent step of forming under bump metallurgy layer **429**. The first barrier layer **427** may be selected to provide

adhesion between the under bump metallurgy layer **429** and the passivation layers **425a** and/or **425b**; to provide adhesion between the under bump metallurgy layer **429** and the interconnection layer **419**; to provide electrical conduction of signals between under bump metallurgy layer **429** and the substrate **421**; and/or to provide an etch selectivity with respect to the first metal layer **423a**. Accordingly, the first barrier layer **427** may be removed from the first metal layer **423a** without significantly damaging the metal layer **423a**.

The conductive under bump metallurgy layer **429** may then be formed on the barrier layer **427** opposite the substrate **421**, the first metal layer **423a**, and the interconnection layer **419**. More particularly, the conductive under bump metallurgy layer **429** may include copper (Cu). A mask layer **431** (such as a layer of photoresist and/or polymer) may be formed on the conductive under bump metallurgy layer **429**, and a hole **433** may be formed in the mask layer **431** to provide a plating template exposing portions of the under bump metallurgy layer **429** offset from the interconnection layer **419**. More particularly, the mask layer **431** may be a layer of photoresist that has been selectively exposed and developed using photolithographic techniques to form the hole **433**.

A second barrier layer **432** (such as a layer of nickel) and a bumping material **435** (such as a tin based solder, gold, and/or copper) may then be selectively formed on portions of the conductive under bump metallurgy layer **429** exposed by the hole **433**. For example, the second barrier layer **432** and the bumping material **435** may be electroplated with the under bump metallurgy layer **429** providing a plating electrode and a current path under the mask **431**. In an alternative, electroless plating may be used so that a current path under the mask is not needed during plating. Other deposition techniques may also be used.

After forming the second barrier layer **432** and the bumping material **435**, the mask **431** can be stripped, for example, using a dry and/or wet process chemistry. As shown in Figure 14, portions of the conductive under bump metallurgy layer **429** not covered by the bumping material **435** and/or the second barrier layer **432** can be removed. More particularly, portions of the conductive under bump metallurgy layer **429** can be removed using an

etch chemistry that removes the conductive under bump metallurgy layer **429** preferentially with respect to the first barrier layer **427**. Accordingly, the first barrier layer **427** may protect the first metal layer **423a** while removing portions of the under bump metallurgy layer **429**. With a conductive under bump metallurgy layer **429** of copper (Cu) and a first barrier layer **427** of titanium-tungsten (TiW), Ammonium Hydroxide may be used to selectively remove the conductive under bump metallurgy layer **429** while maintaining the first metal layer **423a**.

Portions of the first barrier layer **427** not covered by the bumping material **435**, the second barrier layer **432**, and/or remaining portions of the under bump metallurgy layer **429** can then be removed using an etch chemistry that removes the first barrier layer **427** preferentially with respect to the first metal layer **423a**. Accordingly, the first barrier layer **427** may be removed without significantly damaging the first metal layer **423a**. With a first barrier layer 427 of titanium-tungsten (TiW) and a first metal layer 423a of aluminum (Al), portions of the first barrier layer 427 may be removed using a mixture including:

Hydrogen peroxide - 10-20%;
Sulfosalicylic acid - 2-30 grams/liter;
Potassium sulfate - 25-200 grams/liter;
Benzotrizole - 1-10 grams/liter;
Water for makeup;
Temp: 30 to 70 degC; and
pH<7.

The structure of Figure 14 can then be heated so that the bumping material 435 forms a ball while the first metal layer 423a (such as an aluminum layer) is exposed. With a tin based solder bumping material, for example, the bumping material **435** may be fluxed, reflowed, and cleaned to provide the ball of bumping material **435**. With a gold bumping material, the bumping material **435** may be annealed. In an alternative, the bumping material **435** may be bonded to a compatible substrate without first forming a ball.

Accordingly, the bumping material **435** can be used to provide electrical and/or mechanical coupling to another substrate (such as another integrated circuit semiconductor device and/or a printed circuit board) while

the first metal layer **423a** is exposed. Accordingly, the first metal layer **423a** may be burned, cut, probed, and/or wire bonded after forming the bumping material **435** and/or after bonding the bumping material **435** to another substrate.

Figures 15-17 illustrate assemblies of integrated circuit devices according to further embodiments of the present invention. The integrated circuit device of Figure 15 may include a substrate **621** and a passivation layer **625** having a plurality of holes **633** therein with each hole exposing a portion of a respective metal layer **623** (such as an aluminum layer). The device of Figure 15 may also include a plurality of bumps **635** on respective support structures **651**. The integrated circuit device of Figure 15 may thus be provided according to embodiments of the present invention as discussed above with respect to Figures 1-4, with respect to Figures 5-8, with respect to Figures 9-12, and/or with respect to Figures 13-14.

Each support structure **651**, for example, may include a first barrier layer (such as a layer of TiW, TiN, and/or combinations thereof), an under bump metallurgy layer (such as a layer of copper) on the first barrier layer, and a layer of a second barrier layer (such as a layer of nickel). Each bump **635**, for example, may be a tin based solder bump, a gold bump, and/or a copper bump. Moreover, one or more of the bumps **635**, for example, may be on a support structure **651** opposite an input/output pad of the substrate **621** as discussed above with respect to Figures 5-8. In an alternative, one or more of the bumps **635**, for example, may be electrically connected to and offset from a respective input/output pad of the substrate **621** as discussed above with respect to Figures 9-12 and with respect to Figures 13-14. In addition, each of the metal layers **623** exposed through holes **633** in the passivation layer **625**, for example, may be provided as discussed above with respect to Figures 1-4, with respect to Figures 5-8, with respect to Figures 9-12, and/or with respect to Figures 13-14. The passivation layer **625**, for example, may include an inorganic material (such as silicon dioxide and/or silicon nitride) and/or an organic material (such as polyimide).

As shown in Figure 16, a second electronic device including a substrate **711** and bonding pads **715** may be provided for coupling with the device of Figure 15. The device of Figure 16 may be a semiconductor

integrated circuit device including electronic circuits therein. Moreover, the bonding pads **715** may correspond to respective bumps **635** of Figure 15 for bonding therewith. In an alternative, bumps may be provided on the bonding pads **715** in addition to or instead of bumps **635** of Figure 15.

As shown in Figure 17, bonding pads **715** of substrate **711** may be bonded to respective bumps **635** so that substrates **621** and **711** are electrically and mechanically connected. Moreover, the metal layers **623** (such as aluminum layers) may be exposed after providing the bumps **635** and after bonding the substrate **711** using the bumps **635**. The metal layers **623**, for example, may thus be burned, cut, probed, and/or wire bonded after forming the bumps **635** and/or after bonding the bumps **635** to the second substrate **711**. One or more of the metal layers **633**, for example, may be burned using a laser and/or mechanically cut to provide coupling and/or decoupling of redundant and/or faulty circuitry within the substrate **621**. In an alternative, one or more of the metal layers **635** may be probed to test circuitry within the substrate 612. In another alternative, one or more of the metal layers 635 may receive a wire bond to provide electrical coupling between circuitry within the substrate 621 and another electronic substrate and/or device.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

**That which is claimed is:**

1. A method of bumping a substrate including a metal layer thereon wherein the metal layer has an exposed portion, the method comprising:

forming a barrier layer comprising a barrier layer material on the substrate and on the exposed portion of the metal layer;

forming a conductive bump comprising a conductive bump material on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to a surface of the substrate so that the exposed portion of metal layer is free of the conductive bump material; and

after forming the conductive bump, removing the barrier layer from the exposed portion of the metal layer while maintaining a portion of the barrier layer between the conductive bump and the substrate so that the portion of the barrier layer maintained between the conductive bump and the substrate is laterally offset and laterally separated from the exposed portion of the metal layer in the direction parallel to the surface of the substrate and so that the exposed portion of the metal layer is free of the barrier layer material.

2. A method according to claim 1 wherein the substrate comprises an integrated circuit substrate.

3. A method according to claim 1 wherein the metal layer comprises an aluminum layer.

4. A method according to claim 1 wherein the barrier layer comprises a layer of TiW.

5. A method according to claim 1 wherein the metal layer, the barrier layer, and the conductive bump all comprise different materials.

6. A method according to claim 1 further comprising:

before forming the conductive bump, forming a conductive under bump metallurgy layer on the barrier layer; and before removing the barrier layer, removing the conductive under bump metallurgy layer from the barrier layer opposite the metal layer while maintaining a portion of the conductive under bump metallurgy layer

between the conductive bump and the substrate so that the portion of the conductive under bump metallurgy layer maintained between the conductive bump and the substrate is laterally offset and laterally separated from the exposed portion of the metal layer in the direction parallel to the surface of the substrate and so that the exposed portion of the metal layer is free of the conductive under bump metallurgy layer.

7. A method according to claim 6 wherein the conductive under bump metallurgy layer comprises copper.

8. A method according to claim 6 wherein the conductive under bump metallurgy layer and the barrier layer comprise different materials.

9. A method according to claim 6 further comprising:

before forming the conductive bump, forming a second barrier layer on the under bump metallurgy layer wherein the second barrier layer and the under bump metallurgy layer comprise different materials and wherein the second barrier layer is between the conductive bump and the conductive under bump metallurgy layer.

10. A method according to claim 9 wherein the second barrier layer comprises nickel.

11. A method according to claim 10 wherein the under bump metallurgy layer comprises copper.

12. A method according to claim 9 wherein forming the second barrier layer comprises selectively forming the second barrier layer on a portion of the under bump metallurgy layer wherein the second barrier layer is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to the surface of the substrate.

13. A method according to claim 12 wherein forming the conductive bump comprises selectively forming the conductive bump on the second barrier layer laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to the surface of the substrate.

14. A method according to claim 13 wherein selectively forming the second barrier layer and selectively forming the conductive bump comprise selectively forming the second barrier layer and the conductive bump using a same mask.

15. A method according to claim 1 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

16. A method according to claim 1 wherein forming the conductive bump comprises selectively plating the bump on the barrier layer laterally offset and laterally separted from the exposed portion of the metal layer in a direction parallel to the surface of the substrate.

17. A method according to claim 1 wherein the integrated circuit substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein the conductive bump is formed on the barrier layer opposite the input/output pad.

18. A method according to claim 17 wherein the metal layer and the bump pad both comprise aluminum.

19. A method according to claim 1 wherein the substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein after removing the barrier layer from the exposed portion of the metal layer, the conductive bump is electrically coupled to the input/output pad.

20. A method according to claim 19 wherein the metal layer and the input/output pad both comprise aluminum.

21. A method according to claim 19 wherein the conductive bump is formed on the barrier layer opposite the input/output pad.

22. A method according to claim 19 wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate.

23. A method according to claim 1 further comprising:

after removing the barrier layer from the exposed portion of the metal layer, bonding a second substrate to the conductive bump.

24. An electronic device comprising:
a substrate including an exposed metal layer thereon;
a barrier layer on the substrate offset from the exposed metal layer ; and
a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the conductive bump is offset from the metal layer, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

25. An electronic device according to claim 24 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

26. An electronic device according to claim 24 wherein the barrier layer comprises titanium tungsten.

27. An electronic device according to claim 25 wherein the exposed metal layer comprises aluminum.

28. An electronic device according to claim 25 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

29. An electronic device according to claim 24 further comprising a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

30. An electronic device according to claim 24 further comprising:
a second substrate bonded to the conductive bump.

31. An electronic device according to claim 24 further comprising an input/output pad on the integrated circuit substrate wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

32. An electronic device according to claim 31 wherein the input/output pad and the metal layer each comprise aluminum.

33. An electronic device according to claim 31 wherein the conductive bump is on the barrier layer opposite the input/output pad.

34. An electronic device according to claim 31 wherein the conductive bump is offset from the input/output pad.

35. An electronic device according to claim 25 further comprising:

an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.

36. A method of bumping an electronic device comprising a substrate including a metal layer thereon wherein the metal layer has an exposed portion, the method comprising:

forming a barrier layer comprising a barrier layer material on the substrate wherein the barrier layer is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to a surface of the substrate so that the exposed portion of the metal layer is free of the barrier layer material; and

forming a conductive bump comprising a conductive bump material on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the conductive bump is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to the surface of the substrate so that the exposed portion of the metal layer is free of the conductive bump material, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

37. A method according to claim 36 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

38. A method according to claim 36 wherein the barrier layer comprises titanium tungsten.

39. A method according to claim 38 wherein the exposed metal layer comprises aluminum.

40. A method according to claim 38 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

41. A method according to claim 36 further comprising:
forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

42. A method according to claim 36 further comprising:
bonding a second substrate bonded to the conductive bump.

43. A method according to claim 36 wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

44. A method according to claim 43 wherein the input/output pad and the metal layer each comprise aluminum.

45. A method according to claim 43 wherein the conductive bump is on the barrier layer opposite the input/output pad.

46. A method according to claim 43 wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate.

47. A method according to claim 36 further comprising:
an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.

48. A method of bumping an integrated circuit substrate including a metal layer thereon wherein the metal layer has an exposed portion, the method comprising:
forming a barrier layer on a substrate and on the exposed portion of the metal layer;
forming a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is laterally offset and laterally separated from the metal layer in a direction parallel to a surface of the substrate; and

after forming the conductive bump, removing the barrier layer from the exposed portion of the metal layer while maintaining a portion of the barrier layer between the conductive bump and the substrate so that the portion of the barrier layer maintained between the conductive bump and the substrate is laterally separated from the metal layer in a direction parallel to the surface of the substrate.

49. An integrated circuit device comprising:
an integrated circuit substrate;
an exposed metal layer on the integrated circuit substrate;
a barrier layer on the integrated circuit substrate laterally offset from the exposed metal layer ; and
a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is remote from the metal layer.

50. A method according to claim 1 wherein removing the barrier layer further comprises removing the barrier layer from portions of the substrate surrounding the exposed portion of the metal layer.

51. A method according to claim 36 wherein portions of the substrate surrounding the exposed portion of the metal layer are free of the barrier layer material.

52. A method according to claim 48 wherein removing the barrier layer further comprises removing the barrier layer from portions of the substrate surrounding the exposed portion of the metal layer.

53. A method of bumping an electronic device comprising a substrate including a metal layer wherein the metal layer has an exposed portion, the method comprising:
forming a barrier layer comprising a barrier layer material on the substrate wherein the exposed portion of the metal layer and portions of the substrate surrounding the exposed portion of the metal layer are free of the barrier layer material; and
forming a conductive bump comprising a conductive bump material on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the exposed portion of the metal layer and portions of the substrate surrounding the exposed portion of the metal layer are free of the conductive

bump material, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

54. A method according to claim 53 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

55. A method according to claim 53 wherein the barrier layer comprises titanium tungsten.

56. A method according to claim 55 wherein the exposed metal layer comprises aluminum.

57. A method according to claim 55 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

58. A method according to claim 53 further comprising:
forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

59. A method according to claim 53 further comprising:
bonding a second substrate bonded to the conductive bump.

60. A method according to claim 53 wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

61. A method according to claim 60 wherein the input/output pad and the metal layer each comprise aluminum.

62. A method according to claim 60 wherein the conductive bump is on the barrier layer opposite the input/output pad.

63. A method according to claim 60 wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate.

64. A method according to claim 53 further comprising:

an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.