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(54) FOUR-QUADRANT MULTIPLIER

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a four-quadrant multiplier circuit for producing an output signal which is proportional to the product of first and second input signals, comprising a first differential stage with first and second transistors whose common-electrode circuit includes a current source, means for applying the first input signal as a differential signal to the control electrodes of said first and second transistors, a second differential stage with third and fourth transistors whose common-electrode circuit includes the main current path of the first transistor, means for applying the second input signal as a differential signal to the control electrodes of said third and fourth transistors, a third differential stage with fifth and sixth transistors whose common-electrode circuit includes the main current path of the second transistor, the control electrode of the fifth transistor being connected to the control electrode of the fourth transistor and the control electrode of the sixth transistor being connected to the control electrode of the third transistor, and means for combining currents derived from the outputs of transistors of the second and the third differential stage to obtain said output signal.

The accuracy attainable with such a multiplier circuit is limited by several factors. One of these factors is the differences which may exist between the various transistors of the circuit arrangement, with the result that matched transistor pairs are preferably used for the differential stages if the multiplier circuit is built up from discrete components, or if it is constructed in integrated-circuit form optimum equality of the transistors should be aimed at by using very accurate integrated circuit techniques.

A second important factor is that the input signals are converted into the current components utilized in the multiplier circuit by means of a non-linear element, which can introduce undesired distortions, resulting again in product formation errors.

Finally, the base currents of the transistors exhibit variations which, of course, increase as the current gain factors of the transistors decrease. In addition, the various transistors may have mutually different current gain factors, and these gain factors themselves may vary, for example because of temperature fluctuations, thus causing considerable and unpredictable product-formation errors.

It is an object of the invention to reduce the effect of the two last-mentioned factors.

The invention provides a four-quadrant multiplier circuit for producing an output signal which is proportional to the product of first and second input signals, comprising a first differential stage with first and second transistors whose common-electrode circuit includes a current source, means for applying the first input signal as a differential current signal to the control electrodes of said first and second transistors, a second differential stage with third and fourth transistors whose common-electrode circuit includes the main current path of the first transistor, means for applying the second input signal as a differential current signal to the control electrodes of said third and fourth transistors, and a third differential stage with fifth and sixth transistors whose common-electrode circuit includes the main current path of the second transistor, the control electrode of the fifth transistor being connected to the control electrode of the fourth transistor and the control electrode of the sixth transistor being connected to the control electrode of the third transistor, means for combining currents derived from the outputs of transistors of the second and the third differential stage to obtain said output signal, a multiple current mirror having its input current path included in the output current path of the fourth transistor, having a first output current path coupled to first adding means

for forming a first sum current from a current derived from the output of the third transistor and the current in said first output current path, and having a second output current path coupled to second adding means for forming a second sum current from a current derived from the output of the fifth transistor and the current in said second output current path, first negative-feedback means for feeding back the first sum current degeneratively to the input of the first differential stage and second negative-feedback means for feeding back the second sum current degeneratively to the input of the second differential stage.

A "current mirror" is to be understood to mean a d.c. current amplifier for realising a current in an output current path thereof which is in a constant ratio to a current in an input current path thereof for at least a range of values of current in said input current path, which ratio is substantially independent of temperature and supply voltage. In order to achieve this constant ratio the current mirror includes a coupling circuit intercoupling said input and output paths, said coupling circuit having an input current path for carrying at least the main part of any current flowing in one of said amplifier current paths, an output current path for carrying a current at least the main part of which flows through the other of said amplifier paths, a current to voltage converter included in the coupling circuit input current path for converting current in that path into a voltage, and a voltage to current converter included in the coupling circuit output current path for converting said voltage into current in the coupling circuit output current path, the current to voltage converter and the voltage to current converter having substantially similar current-voltage characteristics for at least a range of values of current applied to the current to voltage converter. ("Having substantially similar current-voltage characteristics" means that if the current (I_1)-voltage (V) characteristic of the current to voltage converter is expressed as $I_1=f(V)$, the current (I_2)-voltage (V) characteristic of the voltage to current converter is given by $I_2=af(V)$, in which a is a constant substantially independent of temperature and supply voltage.

A multiple current mirror has more than one such amplifier output current path.

The first negative feedback means may be a direct connection if the signal component present in the first sum current is of a suitable polarity.

It should be noted that the IEEE Journal of Solid State Circuits, August 1970, pages 150-159 describes a four quadrant multiplier circuit in which negative voltage feedback to one input is provided.

Embodiments of the invention will now

be described in more detail, by way of example, with reference to the accompanying digrammatic drawings, in which Figure 1 shows a first embodiment, and Figure 2 shows a second embodiment. Corresponding elements are denoted by the same reference letters and numerals in the two Figures.

The four-quadrant multiplier circuit shown in Figure 1 comprises three differential stages with npn-type transistors 1 and 2, 3 and 4, 5 and 6 respectively, the emitter currents of the transistors 3 and 4 being supplied by transistor 1 and the emitter currents of the transistors 5 and 6 by transistor 2. The emitter currents of these transistors 1 and 2 are, in turn, supplied by a current source I_1 . A first input signal is applied as a differential signal to the bases of the transistors 1 and 2 and a second input signal is applied as a differential signal to the bases of the transistors 3 and 4, which bases are also connected to the bases of the transistors 6 and 5 respectively. The bases of transistor 2 and transistors 4 and 5 are connected to reference voltage points V_{ref1} and V_{ref2} respectively and the input signals x and y are applied as currents to the bases of transistor 1 and transistors 3 and 6 respectively.

As is evident from the Figure, the current supplied by the current source I_1 is distributed between the transistors 3 to 6 in accordance with the magnitudes of the x and y signals. Summation of the output currents of two suitably selected said transistors, for example the output currents of the transistors 3 and 5, gives a current which is proportional to the product xy .

The collector current of transistor 4 is supplied to the input of a first, multiple current mirror S_1 . This current mirror is shown as comprising, by way of example, three pnp-type transistors 12, 13 and 14, whose bases are interconnected, and whose emitters are connected to a sum terminal via resistors R_{12} , R_{13} and R_{14} respectively. Transistor 12 is connected as a diode. This arrangement ensures that a current supplied to transistor 12 is reproduced in the collectors of transistors 13 and 14 with a fixed ratio which is determined by the values of the resistors R_{12} to R_{14} and the areas of the transistors. In the simplest case the transistors and the resistors are identical, so that the two output currents i_{11} , i_{12} of the current mirror S_1 always equal the input current, i.e. equal the collector current of transistor 4.

The collector current of transistor 3 is supplied to the input of a second current mirror S_2 , which is shown, by way of example, as being of the floating type. The input circuit of this current mirror includes an npn-transistor 7 which is connected as a diode and, in series therewith, the emitter-collector path of a pnp-transistor 8. The output circuit of this current mirror includes

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the series-connected main current paths of an npn-transistor 9 and two pnp-transistors 10 and 11, transistor 10 being connected as a diode. The bases of transistors 7 and 9 are interconnected, as are those of the transistors 8 and 10 whilst the base of transistor 11 is connected to the input of the current mirror, i.e. the collector of transistor 8. Because of these interconnections the sum of the base-emitter voltages of the transistors 9 and 10 in the output circuit necessarily equals the sum of the base-emitter voltages of the transistors 7 and 8 in the input circuit, so that if the transistor geometries are equal the output current will always equal the input current.

The collector current of transistor 5 is applied to the input of a third current mirror S_3 , which is identical to the current mirror S_2 , consists of transistors 15 to 19. A first sum current i_{s1} is generated by connecting the output of the current mirror S_2 to an output of the current mirror S_1 , and a second sum current i_{s2} is generated by connecting the output of the current mirror S_3 to the remaining output of the current mirror S_1 . The first sum current i_{s1} is applied to the input of a current mirror S_{10} which consists of a diode-transistor configuration 20 and 21 and whose output is connected to the base of transistor 1 of the first differential stage. The second sum current i_{s2} is applied directly to the base of transistor 3 of the second differential stage. Moreover, d.c. components derived from current sources I_2 and I_3 are applied to the bases of transistors 1 and transistor 3 respectively.

The magnitudes of the resulting negative-feedback currents can be calculated in a simple manner. Assuming that the current source I_1 supplies a current $4I$, the collector currents i_3 to i_6 of the transistors 3 to 6 respectively may initially be expressed in known manner by:

$$\begin{aligned} i_3 &= (1+x+y+xy)I \\ i_4 &= (1+x-y-xy)I \\ i_5 &= (1-x-y+xy)I \\ i_6 &= (1-x+y-xy)I \end{aligned} \quad (1)$$

Assuming that all the current mirrors reproduce the currents applied to their inputs at their outputs with a gain of unity, the output currents i_{21} and i_{31} respectively of the current mirrors S_2 and S_3 equal i_3 and i_5 respectively, and each of the two output currents i_{11} , i_{12} of the current mirror S_1 equals i_4 . This means that the first sum current i_{s1} which comprises the output current i_{21} of the current mirror S_2 and the collector current i_{11} of transistor 13 of the current mirror S_1 equals $i_3+i_4=(1+x)2I$, so that, in addition

to a d.c. component, this sum current initially only contains an x-component. By applying this sum current to the base of transistor 1, via the current mirror S_{10} , a negative feedback current which equals $-(1+x)2I$ is obtained at this input, thus providing full negative feedback of the x-component. The d.c. component $-2I$ of this negative-feedback current is supplied by the current source I_2 , but may, of course, alternatively be included in the input current.

The second sum current i_{s2} which is generated by summation of the output current i_{31} of the current mirror S_3 and the collector current i_{12} of transistor 14, initially equals $i_4+i_5=(1-y)2I$, so that this sum current primarily only contains the y-component in addition to the d.c. component. Full negative feedback of this y-component is obtained by applying said sum current directly to the base of transistor 3. The d.c. component $2I$ of this negative-feedback current is supplied by the current source I_3 .

Thus the provision of current mirrors, including the multiple current mirror S_{11} , permits the application of negative feedback to both inputs (x and y) of the multiplier circuit.

There are several alternatives to the described method of generating the desired sum currents. For example, it is possible to construct the current mirror S_1 as a floating current mirror similar to S_2 and S_3 . These floating current mirrors such as S_2 already comprise a first output (the collector of transistor 11), a second output (the collector of transistor 9), and sometimes a third output (the collector of transistor 7). If such a floating current mirror is used for the current mirror S_1 , its first output may again be connected to the first output of the current mirror S_2 in order to obtain the first sum current. However, in order to obtain the second sum current the second output of said floating current mirror may be connected to the collector of transistor 5, the second sum current thus generated being then processed with the aid of current mirror S_3 . It will be obvious that in this case the levels between the various components should be suitably adapted.

As a second alternative the x signal may be applied to the base of transistor 2 instead of transistor 1, the base of transistor 1 then being connected to the reference voltage V_{ref1} . The first sum current i_3+i_4 will then equal $(1-x)2I$, so that this sum current can be applied directly to the base of transistor 2 in order to obtain the desired negative feedback, thus making the additional current mirror S_{10} superfluous.

The desired product can be obtained simply by adding the collector current of transistor 9 of the current mirror S_2 to the collector current of transistor 17 of current mirror S_3 , yielding a current $i_5+i_6=(1+xy)2I$.

The four-quadrant multiplier circuit of Figure 2 again comprises three differential stages including transistors 1 to 6 to which the input signals x and y are applied in a corresponding manner. However, now each of the collector currents i_3 to i_6 of the transistors 3 to 6 is individually applied to a multiple current mirror. As the four current mirrors S_1 to S_4 are identical, only the circuit arrangement of the current mirror S_1 will be described in more detail.

The input current of the current mirror S_1 , the collector current of transistor 4, is applied to a resistor 44. One end of this resistor 44 is connected to the sum terminal of the current mirror and its other end to the base of an npn-transistor 41 which is connected as an emitter follower. A current source I_{41} supplies a quiescent current to transistor 41, the collector of which is connected to the positive terminal $+V_B$ of the supply. The emitter of this transistor 41 is, in turn, connected to the bases of two pnp-transistors 42 and 43, whose emitters are connected to the sum terminal of the current mirror via resistors 45 and 46, respectively. The collectors of the transistors 42 and 43 constitute the two outputs of the current mirror and supply currents which are in a fixed ratio to the input current, which ratio is determined by the values of the resistors 44, 45 and 46. Despite the generally low current amplification factor of the npn-transistors, the current mirror shown can operate very accurately.

To obtain the desired negative-feedback currents the sum of an output current i_{11} of the current mirror S_1 and an output current i_{21} of the current mirror S_2 is produced first of all, similarly to the circuit arrangement of Figure 1, yielding a sum current $i_3 + i_4 = (1+x) 2I$. After processing in a current mirror S_{10} this results in the application of a negative-feedback current $-(1+x) 2I$ to the base of transistor 1. A second sum current i_{32} is again generated by summation of an output current i_{31} of the current mirror S_3 and the second output current i_{12} of the current mirror S_1 , resulting in a current $i_4 + i_5 = (1-y) 2I$, which is applied directly to the base of transistor 3.

However, the circuit arrangement of Figure 2 also produces a third and a fourth sum current. The fourth sum current i_{34} is obtained by summation of the second output current i_{32} of the current mirror S_3 and the second output current i_{42} of the current mirror S_4 and equals $i_5 + i_6 = (1-x) 2I$. This sum current is applied directly to the base of transistor 1, thus providing negative feedback for the x -component. The overall negative-feedback current fed to the base of transistor 1 is the sum of the first negative-feedback current from the output of the current mirror

S_{10} and the last-mentioned negative feedback current:

$$-(1+x) 2I + (1-x) 2I = -4xI,$$

so that the d.c. component is fully compensated for.

The same is achieved at the y -input by applying the third sum current i_{33} , which is the sum of the second output current i_{22} of the current mirror S_2 and the first output current i_{41} of the current mirror S_4 to the base of transistor 3 via a current mirror S_{11} .

The desired product current can be obtained in a very simple manner by interconnecting the sum terminals of the current mirrors S_2 and S_3 , which results in an overall current of $(1+xy) 6I$. A second product current $(1-xy) 6I$ can be obtained by interconnecting the sum terminals of the current mirrors S_1 and S_4 .

As alternative the input signals can be supplied to the arrangement symmetrically, in such a way that the $-x$ -component of the balanced x -signal is applied to the base of transistor 2 instead of the reference signal V_{ref1} and the $-y$ -component of the balanced y -signal is applied to the base of transistor 4 instead of the reference signal V_{ref2} . The first sum current can then be applied to the base of transistor 2 directly, so that the current mirror S_{10} can be dispensed with, and the third sum current can be applied to the base of transistor 4 directly so that current mirror S_{11} becomes superfluous. Thus, the negative-feedback currents can also be applied to the two inputs in a balanced manner in this way. However, if this is done measures will have to be taken again to compensate for the d.c. component in the negative feedback currents.

It will be obvious that other forms of current mirror may be used, if desired. Moreover, the input signals may be in the form of input voltages which are fed to resistors connected to the bases of the relevant transistors.

WHAT WE CLAIM IS:—

1. A four-quadrant multiplier circuit for producing an output signal which is proportional to the product of first and second input signals, comprising a first differential stage with first and second transistors whose common-electrode circuit includes a current source, means for applying the first input signal as a differential current signal to the control electrodes of said first and second transistors, a second differential stage with third and fourth transistors whose common-electrode circuit includes the main current path of the first transistor, means for applying the second input signal as a differential current signal to the control electrodes of said third and fourth transistors, and a third differ-

The four-quadrant multiplier circuit of Figure 2 again comprises three differential stages including transistors 1 to 6 to which the input signals x and y are applied in a corresponding manner. However, now each of the collector currents i_3 to i_6 of the transistors 3 to 6 is individually applied to a multiple current mirror. As the four current mirrors S_1 to S_4 are identical, only the circuit arrangement of the current mirror S_1 will be described in more detail.

The input current of the current mirror S_1 , the collector current of transistor 4, is applied to a resistor 44. One end of this resistor 44 is connected to the sum terminal of the current mirror and its other end to the base of an npn-transistor 41 which is connected as an emitter follower. A current source I_{41} supplies a quiescent current to transistor 41, the collector of which is connected to the positive terminal $+V_B$ of the supply. The emitter of this transistor 41 is, in turn, connected to the bases of two pnp-transistors 42 and 43, whose emitters are connected to the sum terminal of the current mirror via resistors 45 and 46, respectively. The collectors of the transistors 42 and 43 constitute the two outputs of the current mirror and supply currents which are in a fixed ratio to the input current, which ratio is determined by the values of the resistors 44, 45 and 46. Despite the generally low current amplification factor of the npn-transistors, the current mirror shown can operate very accurately.

To obtain the desired negative-feedback currents the sum of an output current i_{11} of the current mirror S_1 and an output current i_{21} of the current mirror S_2 is produced first of all, similarly to the circuit arrangement of Figure 1, yielding a sum current $i_3 + i_4 = (1+x)2I$. After processing in a current mirror S_{10} this results in the application of a negative-feedback current $-(1+x)2I$ to the base of transistor 1. A second sum current i_{32} is again generated by summation of an output current i_{31} of the current mirror S_3 and the second output current i_{12} of the current mirror S_1 , resulting in a current $i_4 + i_5 = (1-y)2I$, which is applied directly to the base of transistor 3.

However, the circuit arrangement of Figure 2 also produces a third and a fourth sum current. The fourth sum current i_{34} is obtained by summation of the second output current i_{32} of the current mirror S_3 and the second output current i_{42} of the current mirror S_4 and equals $i_5 + i_6 = (1-x)2I$. This sum current is applied directly to the base of transistor 1, thus providing negative feedback for the x -component. The overall negative-feedback current fed to the base of transistor 1 is the sum of the first negative-feedback current from the output of the current mirror

S_{10} and the last-mentioned negative feedback current:

$$-(1+x)2I + (1-x)2I = -4xI,$$

so that the d.c. component is fully compensated for.

The same is achieved at the y -input by applying the third sum current i_{33} , which is the sum of the second output current i_{22} of the current mirror S_2 and the first output current i_{11} of the current mirror S_1 , to the base of transistor 3 via a current mirror S_{11} .

The desired product current can be obtained in a very simple manner by interconnecting the sum terminals of the current mirrors S_2 and S_3 , which results in an overall current of $(1+xy)6I$. A second product current $(1-xy)6I$ can be obtained by interconnecting the sum terminals of the current mirrors S_1 and S_4 .

As alternative the input signals can be supplied to the arrangement symmetrically, in such a way that the $-x$ -component of the balanced x -signal is applied to the base of transistor 2 instead of the reference signal V_{ref1} and the $-y$ -component of the balanced y -signal is applied to the base of transistor 4 instead of the reference signal V_{ref2} . The first sum current can then be applied to the base of transistor 2 directly, so that the current mirror S_{10} can be dispensed with, and the third sum current can be applied to the base of transistor 4 directly so that current mirror S_{11} becomes superfluous. Thus, the negative-feedback currents can also be applied to the two inputs in a balanced manner in this way. However, if this is done measures will have to be taken again to compensate for the d.c. component in the negative feedback currents.

It will be obvious that other forms of current mirror may be used, if desired. Moreover, the input signals may be in the form of input voltages which are fed to resistors connected to the bases of the relevant transistors.

WHAT WE CLAIM IS:—

1. A four-quadrant multiplier circuit for producing an output signal which is proportional to the product of first and second input signals, comprising a first differential stage with first and second transistors whose common-electrode circuit includes a current source, means for applying the first input signal as a differential current signal to the control electrodes of said first and second transistors, a second differential stage with third and fourth transistors whose common-electrode circuit includes the main current path of the first transistor, means for applying the second input signal as a differential current signal to the control electrodes of said third and fourth transistors, and a third differ-



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ential stage with fifth and sixth transistors whose common-electrode circuit includes the main current path of the second transistor, the control electrode of the fifth transistor being connected to the control electrode of the fourth transistor and the control electrode of the sixth transistor being connected to the control electrode of the third transistor, means for combining currents derived from the outputs of transistors of the second and the third differential stage to obtain said output signal, a multiple current mirror having its input current path included in the output current path of the fourth transistor, having a first output current path coupled to first adding means for forming a first sum current from a current derived from the output of the third transistor and the current in said first output current path, and having a second output current path coupled to second adding means for forming a second sum current from a current derived from the output of the fifth transistor and the current in said second output current path, first negative-feedback means for feeding back the first sum current degeneratively to the input of the first differential stage and second negative-feedback means for feeding back the second sum current degeneratively to the input of the second differential stage.

2. A circuit as claimed in Claim 1, wherein the first adding means includes a second current mirror whose input current path is included in the output current path of the third transistor and whose output current path is connected to the first output current path of the current mirror of Claim 1 to form the first sum current, and wherein the second adding means includes a third current mirror whose input current path is included in the output current path of the fifth transistor and whose output current path is connected to the second output current path of the current mirror of Claim 1 to produce the second sum current.

3. A circuit as claimed in Claim 2, wherein the second current mirror is a multiple current mirror having a further output current path which is coupled to third adding means for forming a third sum current from a current derived from the output of the sixth transistor and the current in the further output current path of the second current mirror, the circuit including third feedback means for feeding back said third sum current degeneratively to the input of the second differential stage.

4. A circuit as claimed in Claim 2 or 3 wherein the third current mirror is a multiple current mirror having a further output current path which is coupled to further adding means for forming a further sum current from a current derived from the output of

the sixth transistor and the current in the further output current path of the third current mirror, the circuit including further negative feedback means for feeding back said further sum current degeneratively to the input of the first differential stage.

5. A circuit as claimed in Claim 3, or in Claim 4 when appended to Claim 3, wherein the third adding means includes a fourth current mirror whose input current path is included in the output current path of the sixth transistor and whose output current path is connected to the further current path of the second current mirror to form the third sum current.

6. A circuit as claimed in Claim 4, or in Claim 5 when appended to Claim 4, wherein the further adding means includes a current mirror whose input current path is included in the output current path of the sixth transistor and whose output current path is connected to the further output current path of the third current mirror to form the further sum current.

7. A circuit as claimed in Claim 5 when appended to Claim 4, wherein the fourth current mirror is a multiple current mirror and is also included in the further adding means, a further output current path of said fourth current mirror being connected to the further output current path of the third current mirror to form the further sum current.

8. A circuit as claimed in Claim 3, or Claim 4, 5, 6 or 7 when appended to Claim 3, wherein the second and third negative-feedback means are connected to the control electrode of one and the same transistor of the second differential stage, one of these said negative-feedback means establishing a direct connection between the relevant adding means and said control electrode, and the other of these said negative-feedback means including a current mirror for inverting the relevant sum current.

9. A circuit as claimed in Claim 4 or in any of Claims 5 to 8 when appended to Claim 4, wherein the first and the further negative-feedback means are connected to the control electrode of one and the same transistor of the first differential stage, one of these said negative-feedback means establishing a direct connection between the relevant adding means and this said control electrode, and the other of these said negative-feedback means including a current mirror for inverting the relevant sum current.

10. A four-quadrant multiplier circuit as claimed in Claim 7, including means for applying the two input signals to the first and second differential stages in a balanced manner, the two negative-feedback means coupled to each differential stage being coupled one to each of the two said transistors of that stage.



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11. A four-quadrant multiplier circuit as claimed in any of the preceding Claims, manufactured as an integrated-circuit.

5 12. A four quadrant multiplier circuit substantially as described herein with reference to Figure 1 or Figure 2 of the drawings.

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