

MULTILAYER PRINTED-CIRCUIT BOARD AND METHOD OF FABRICATING
THE MULTILAYER PRINTED-CIRCUIT BOARD

1. Title of the Invention:

Multilayer printed-circuit board and method of fabricating
the multilayer printed-circuit board

2. Detailed Description of the Invention:

[Field of the invention]

The present invention relates to a multilayer circuit board and a method of fabricating the multilayer circuit board, and more particularly to a multilayer printed-circuit board where a plurality of wires in different layers are electrically connected by through-holes and a method of fabricating the multilayer printed-circuit board.

[Background art]

As electronic equipment becomes a small size and highly efficient, the printed-circuit board must have a larger number of wires in a limited space. For the layout of the wiring, it is effective to increase the number of circuit layers of a printed-circuit board and make the board into a multilayer circuit board. A plurality of circuit layers such as this are connected with each other through contact holes.



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The process of fabricating a conventional multilayer circuit board will be described in reference to Figure 1. Figure 1 is a process diagram showing a method of fabricating a conventional printed-circuit board. A conductor 11 is first formed on a substrate 10 having an insulation layer (Figure 1(a)). Then, photoresist 12 is blanket-coated on the conductor 11 and is selectively exposed to develop the resist (Figure 1(b)). The conductor 11 is selectively etched to form a desired lower wiring 13 (Figure 1(c)) and then the remaining photoresist 12 is removed (Figure 1(d)). Next, on this lower wiring 13 formed, a photosensitive insulation resin layer 14 is deposited (Figure 1(e)). This resin layer 14 is selectively exposed and then is etched to form a contact hole 15, and the lower wiring 13 is exposed (Figure 1(f)). Furthermore, with a film formation technique such as electroless plating, deposition, and sputtering, an upper wiring 16 is formed on the contact hole 15 and the lower wiring 13 (Figure 1(g)). By repeatedly performing these steps of forming the insulation layer and the wiring layer, multilayer wiring is formed on the substrate.

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The printed-circuit board formed in this way is to be connected to some circuit through a metal wire such as a gold wire. This is achieved by bonding a gold wire on the board. Figure 2 is a diagram showing the state where the gold wire was bonded on the printed-circuit board. As shown in Figure 2(a), a wire 16 has been connected to a predetermined area of an upper wiring 15 formed on a photosensitive insulation resin layer 14, that is, to a connection area. In normal wire bonding, the wire 16 is pressed against the connection area with a weight of about 50 g through 150 g, and at the same time, ultrasonic vibration is applied to the connection area so that the gold wire is fixed to

the connection area by thermocompression bonding.

[Problems to be solved by the invention]

As the aforementioned photosensitive resin layer, there is, for example, epoxy resin having photosensitivity. Typically, PROBIMER-52 made of liquid photosensitive epoxy resin (made by Japan Chiba Gaigi) can be used. Although there are some other materials, these photosensitive resin layers are all susceptible to deformation by high temperature or high pressure. Therefore, in bonding the wire 16 to the bonding pad 15, there are some cases where the photosensitive resin layer 14 is softened by thermocompression bonding through application of heat and application of pressure and therefore a depressed portion occurs in the direction where the wire 16 is pressed, as shown by reference character A in Figure 2(a). In addition to the softening caused by heat or pressure, there is the possibility that the depressed portion will be amplified by the ultrasonic vibration applied to the bonding pad 15, when bonding is performed.

If wire bonding is performed in this state, there will be possibility that, at the portion B clamped by the capillary head 17 of a bonding machine and the edge of the depressed portion A, the wire 16 will be excessively pressed locally and cut, as shown in Figure 2(b). On the other hand, if the temperature, applied when bonding is performed, is set to a low temperature in order to prevent such a depressed portion of the photosensitive resin layer 14, then there will be the problem that a sufficient connection strength cannot be obtained between the wire and the pad and therefore a reduction in reliability of the connection will be caused.

Accordingly, an object of the present invention is to prevent the photosensitive resin layer from being depressed by external heat, pressure, or ultrasonic vibration.

Another object of the present invention is to perform bonding without reducing the strength of the connection between the wire and the pad.

[Summary of the invention]

To achieve the above objects and in accordance with one aspect of the present invention, there is provided a multilayer circuit board having a substrate, a first conductive circuit layer formed on the substrate, a photosensitive insulation layer formed on the first conductive circuit layer, and a second conductive circuit layer formed on the photosensitive insulation layer and electrically connected to the first conductive circuit layer through a plurality of contact holes formed in the photosensitive insulation layer. In the multilayer circuit board, the second conductive circuit layer has a wiring area where a plurality of wires are arranged and a pad area to which external heat or pressure is applied in order to connect a conductive wire, and the thickness of the second conductive circuit layer in at least part of the pad area is greater than that of the second conductive circuit layer in the wiring area.

In accordance with another aspect of the present invention, there is provided a multilayer circuit board having a substrate, a first conductive circuit layer formed on the substrate, a photosensitive insulation layer formed on the first conductive circuit layer, and a second conductive circuit layer formed on the photosensitive insulation layer and electrically connected to the first conductive circuit layer through a plurality of contact

holes formed in the photosensitive insulation layer. In the multilayer circuit board, the second conductive circuit layer has a wiring area where a plurality of wires are arranged and a pad area to which external heat or pressure is applied in order to connect a conductive wire, and the thickness of the photosensitive insulation layer existing under at least a partial area of the pad area is less than that of the photosensitive insulation layer existing under the wiring area, excluding the contact holes.

In accordance with still another aspect of the present invention, there is provided a method of fabricating a multilayer circuit board, comprising the steps of forming a first conductive circuit layer having a predetermined wiring pattern on a substrate; forming a photosensitive insulation layer on the first conductive circuit layer; exposing the photosensitive insulation layer so that, in a contact-hole area where a contact hole is formed, a first hole is formed in the photosensitive insulation layer, the first hole having a depth of a degree that the first conductive circuit layer is exposed; in at least part of a pad area where a pad is formed, forming a second hole in the photosensitive insulation layer, the second hole having a depth of a degree that the first conductive circuit layer is not exposed; in at least the contact-hole area and the pad area, selectively forming a second conductive circuit layer; and bonding a conductive wire to the second conductive circuit layer in the pad area.

[Operation]

According to the aforementioned invention, in the area where the bonding pad is formed, a photosensitive insulation layer does not exist in at least a portion which easily gets high temperature to a degree that a photosensitive insulation layer is softened by application of heat, and some other material less susceptible to softening is provided. Therefore, an occurrence of depression caused by softening is difficult.

[Preferred embodiment]

A preferred embodiment of the present invention will hereinafter be described. Figure 3 is a process diagram showing a method of fabricating a multilayer circuit board having two circuit layers.

First, a blanket metal layer 32 of copper is formed on an organic substrate 31 by using either a deposition method, a sputtering method, or an electroless plating method (Figure 3(a)).

This metal layer 32 is patterned into a predetermined wiring pattern (Figure 3(b)). This is performed by forming a patterned photoresist on the metal layer 32.

An insulation layer 33 made of photosensitive resin is coated on the metal layer 32. Then, the photosensitive insulation layer 33 is exposed so that, at an area 35, a hole 34 is formed in the photosensitive insulation layer 33. The hole 34 has a depth of a degree that the lower circuit layer 32 is exposed. Next, a hole 37 is formed in the photosensitive insulation layer 33 at part of an area 36, and the hole 37 has a depth of a degree that the lower circuit layer 32 is not exposed (Figure 3(c)). The area 35

is an area for forming a contact hole through which the lower circuit layer 32 is electrically connected to an upper circuit layer 38 which is formed in a subsequent step. The area 37 is an area for forming a connection pad which is formed in a subsequent step, and a wire is connected to the connection pad. The holes 34 and 37 with different depths may be formed by two steps, or they may be formed at the same time by a single step. In the case where the holes are formed in two steps, either hole is first formed with predetermined exposure conditions and a predetermined mask and then the other hole differing in depth is formed by changing the exposure conditions and the mask. In the case where the holes are formed at the same time in a single step, the diameter of the deeper hole 37 is formed so as to become smaller than that of the shallower hole 34. Because the diameter and the depth of the hole would be in proportion to each other even if the exposure conditions were the same, the depth of the hole could be controlled by varying the size of the hole diameter. If this nature is used, it will be possible to form diameters differing in depth in the same step.

As shown in Figure 3(d), the upper circuit layer 38 with a thickness reaching a predetermined leveling position C is formed on the entire surface. This circuit layer 38, as with the metal layer (lower circuit layer) 32, can be formed by using a film formation method such as an electric plating method. Thereafter, the surface of the circuit layer 38 is removed so that the thickness of the circuit layer 38 attains to the leveling position C (Figure 3(d)). If the thickness of the circuit layer 38 does not attain to the leveling position C in this step, a depressed portion D will remain even if the surface of the circuit layer were removed in the step of forming a connection

pad, and consequently, the possibility may occur that a flat connection pad cannot be obtained. If the depressed portion D remains in this way, then the connection strength of the wiring bonding in a postprocess will be reduced. Therefore, in order to prevent an occurrence of a depressed portion D such as this, it is necessary that the hole 37 is plated so as to be filled up. Then, a leveling step of removing the surface of the plated layer is carried out in order to get rid of the depressed portion D and make the surface of the connection pad 40 flat.

The upper circuit layer 38 is patterned (Figure 3(e)). With this, a contact hole 39 is formed in the area 34. Also, the connection pad 40 is formed in the area 36. Furthermore, wiring areas (not shown) are formed.

Finally, the multilayer circuit board is completed by bonding a gold wire to the connection pad 40.

Figure 4 is an enlarged sectional view showing the area 37 of the multilayer circuit board formed in this way. The metal layer 32, patterned into a predetermined wiring pattern, has been formed on the organic substrate 31. Then, the insulation layer 33 composed of the photosensitive organic resin has been formed on the metal layer 32. In the area 37, the connection pad 40 whose surface is flat has been formed on the photosensitive insulation layer 33. The connection pad 40 has been formed on the hole 37 by the aforementioned method. Therefore, the thickness of the connection pad 40 in the area 43 where a gold wire 42 has been connected, that is, the thickness l_1 of the upper circuit layer is greater than the thickness l_2 of the circuit layer in the

wiring area 41 where an upper wiring 44 has been formed.

In other words, even in at least part of the area where the connection pad 40 was formed, the thickness m_1 of the photosensitive insulation layer 33 existing under the area 43 to which external heat and pressure are applied has become less than the thickness m_1 of the photosensitive insulation layer 33 existing under the wiring area 41.

With a constitution such as this, at the area where the pad is formed, the hole 37 is formed, whereby an upper circuit layer exists in at least the area 43 which attains to a temperature of a degree that the photosensitive insulation layer is softened by application of heat. The material of the circuit layer existing in the hole 37, as compared with the photosensitive insulation layer, is a material which is not easily deformed by heat and also has a strong resistance to the pressure and ultrasonic vibration at the time of bonding. Therefore, even in a case where a wire is bonded to the area 43, the area 43 is not easily depressed. In addition, the circuit layer composed of this material makes contact with the photosensitive insulation layer through a curved surface and the surface area of the contacted portion is large. Therefore, because the pressure applied to the area 43 is distributed, the stress of the insulation layer per unit area is reduced and thus the insulation layer of this contacted portion becomes less susceptible to deformation.

While the circuit board with two circuit layers has been described in the aforementioned embodiment, it is obvious that the present invention is applicable to a board having three or

more circuit layers. If the organic substrate 31 shown in Figs. 3 and 4 is considered to be a photosensitive insulation layer having the same material as the insulation layer 33 and it is assumed that an organic substrate exists under the insulation layer, then the description of Figs. 3 and 4, as it is, will hold true of a circuit board having three or more circuit layers. Note that the circuit board may be constructed such that, under at least the area 43 which is part of the area where the bonding pad 40 was formed, a lower metal layer 32 exists through the insulation layer 33. In a case where the organic substrate 31 is replaced with a photosensitive insulation layer, that is, in a structure having three or more circuit layers, a metal layer 32 such as this exists under the connection pad. This metal layer can effectively prevent the heat, pressure, or vibration applied to the connection pad from being transmitted to the insulation layer existing under the metal layer 32. Therefore, the deformation of the insulation layer existing under this metal layer 32 can be suppressed.

Furthermore, while it has been described in the aforementioned embodiment that the hole 37 is filled up with the upper circuit layer itself, the hole may be filled up with an additional material having a strong resistance to heat and the connection pad may be formed on the material by a circuit layer. In addition, the hole 37, as with the hole 34, can be formed so that it has a depth ($m_1 = 0$) of a degree that the lower circuit layer 32 is exposed. Even in this case, an occurrence of depression can be effectively prevented, but attention must be paid so that the lower circuit layers 32 are not connected with each other and that an occurrence of a dead space can be maximally suppressed.

While, in the aforementioned embodiment, the bonding pad to which a bonding wire is connected has been shown as an example of an area to which external heat or pressure is applied, the present invention is not limited to this area but is widely applicable to an area where external heat or pressure is applied. The pad area in the present invention is used in a broad sense including such an area.

[Advantages of the invention]

Thus, in the present invention, the depression of the photosensitive insulation layer can be effectively prevented and it becomes possible to easily perform bonding without reducing the strength of the connection between the wire and the pad.

3. Brief Description of the Drawings:

Figure 1 is a process diagram showing a method of fabricating a conventional printed-circuit board;

Figure 2 is a diagram showing the state where a gold wire was bonded on the printed-circuit board;

Figure 3 is a process diagram showing a method of fabricating a multilayer circuit board of the present invention; and

Figure 4 is an enlarged sectional view of the connection pad area of the multilayer circuit board.

[Description of symbols]

31 ... Organic substrate

32 ... Metal layer

- 33 ... Photosensitive insulation layer
- 40 ... Connection pad
- 42 ... Gold wire
- 44 ... Wiring

4. Claims:

(1) A multilayer circuit board having a substrate,

a first conductive circuit layer formed on said substrate,

a photosensitive insulation layer formed on said first conductive circuit layer, and

a second conductive circuit layer formed on said photosensitive insulation layer and electrically connected to said first conductive circuit layer through a plurality of contact holes formed in said photosensitive insulation layer,

said second conductive circuit layer having a wiring area where a plurality of wires are arranged and a pad area to which external heat or pressure is applied, the thickness of said second conductive circuit layer at least in part of said pad area being greater than that of said second conductive circuit layer in said wiring area.

(2) A multilayer circuit board having a substrate,

a first conductive circuit layer formed on said substrate,

a photosensitive insulation layer formed on said first conductive circuit layer, and

a second conductive circuit layer formed on said photosensitive insulation layer and electrically connected to said first conductive circuit layer through a plurality



of contact holes formed in said photosensitive insulation layer,

said second conductive circuit layer having a wiring area where a plurality of wires are arranged and a pad area to which external heat or pressure is applied, the thickness of said photosensitive insulation layer existing at least under a partial area of said pad area being less than that of said photosensitive insulation layer existing under said wiring area, excluding said contact holes.

(3) A multilayer circuit board having a substrate,

a first conductive circuit layer formed on said substrate,

a photosensitive insulation layer formed on said first conductive circuit layer, and

a second conductive circuit layer formed on said photosensitive insulation layer and electrically connected to said first conductive circuit layer through a plurality of contact holes formed in said photosensitive insulation layer,

said second conductive circuit layer having a wiring area where a plurality of wires are arranged and a pad area to which a conductive wire is connected, the thickness of said second conductive circuit layer at least in part of said pad area being greater than that of said second conductive circuit layer in said wiring area.

(4) A multilayer circuit board having a substrate,



a first conductive circuit layer formed on said substrate,

a photosensitive insulation layer formed on said first conductive circuit layer, and

a second conductive circuit layer formed on said photosensitive insulation layer and electrically connected to said first conductive circuit layer through a plurality of contact holes formed in said photosensitive insulation layer,

said second conductive circuit layer having a wiring area where a plurality of wires are arranged and a pad area where a pad is formed, to which a conductive wire is connected, the thickness of said photosensitive insulation layer existing at least under a partial area of said pad area being less than that of said photosensitive insulation layer existing under said wiring area, excluding said contact holes.

- (5) The multilayer circuit board as set forth in Claim 1, 2, 3, or 4, wherein a surface shape of said second conductive circuit layer in said pad area is flat.
- (6) The multilayer circuit board as set forth in Claim 1, 2, 3, or 4, wherein said first conductive circuit layer exists under at least a partial area of said pad area.
- (7) A method of fabricating a multilayer circuit board, comprising the steps of:

forming a first conductive circuit layer having a predetermined wiring pattern on a substrate;



forming a photosensitive insulation layer on said first conductive circuit layer;

exposing said photosensitive insulation layer so that, in a contact-hole area where a contact hole is formed, a first hole is formed in said photosensitive insulation layer, the first hole having a depth of a degree that said first conductive circuit layer is exposed;

at least in part of a pad area where a pad is formed, forming a second hole in said photosensitive insulation layer, the second hole having a depth of a degree that said first conductive circuit layer is not exposed;

in at least said contact-hole area and said pad area, selectively forming a second conductive circuit layer; and

bonding a conductive wire to said second conductive circuit layer in said pad area.

- (8) The method of fabricating a multilayer circuit board, as set forth in Claim 7, further comprising a step of removing a surface of said second conductive circuit layer in order to make said pad area flat.
- (9) The method of fabricating a multilayer circuit board, as set forth in Claim 7 or 8, wherein a diameter of said second hole is formed so as to be made smaller than that of said first hole.
- (10) The method of fabricating a multilayer circuit board, as set forth in Claim 7 or 8, wherein said first and second holes different in depth are formed in the same step by



making a diameter of said second hole smaller than that of said first hole.

