

A CARRIER CANCELLATION SYSTEM

Field of the Invention

This invention relates to a carrier cancellation system that is configured to generate a cancellation signal having an amplitude and phase that is almost equal to the amplitude and phase of a received carrier signal thereby effectively cancelling the carrier signal. The system is able to achieve such a close match between the amplitudes and phases of the two signals through the use of an initialized logic control module that was pre-initialized using a dual iterative approach to search for an optimal starting phase entry and an optimum gain entry which are then used to generate the cancellation signal.

Background

Near Field Communication (NFC) is an emerging communication technique that has been widely implemented in smartphones in recent years. NFC is advantageous as it is extremely easy and convenient to use in various real world applications such as in mobile payments, verifying a user's identity, and etc. whereby a large part of this convenience is due to the wide spread adoption of Wi-Fi/Bluetooth etc. especially in urban areas. In short, it is predicted by those skilled in the art that NFC has tremendous market value as it may be easily deployed in future Internet-of-Things (IoT) devices, in smart homes, and in smart city environments.

When a NFC device is operating in its reader mode, the sensitivity of the reader's receiver is limited by the carrier signals that was transmitted by the NFC device. This is illustrated in Figure 1 which shows the NFC communication that takes place between NFC device 102 and NFC tag 104. When NFC device 102 is operating in reader mode, device 102 will initiate a field and will send carrier signals 110 to NFC tag 104. When NFC tag 104 replies to NFC device 102, tag 104 will apply load modulation to the received carrier signal to modulate a subcarrier signal onto carrier signal 110. The resulting load modulated signal 115 will then be sent back to NFC device 102.

A metric that is commonly used to describe the proportion of amplitude of subcarrier signal to that of the carrier signal is the Modulation Index (MI) metric whereby MI is defined as,

$$MI = \frac{p - v}{p + v}$$

where p is defined as the peak of load modulated signal 115 and v is defined as the valley of load modulated signal 115. It is easier for NFC device 102 in reader mode to process a load modulated signal when the MI is high however, when NFC device 102 is operating in its reader mode, the MI of the interaction between device 102 and tag 104 is typically very small as tag 104 is not provided with a power source.

The MI will not be significantly improved after the modulated signal is amplified by device 102 as both carrier signal and subcarrier signals are amplified together. The amplitude of the subcarrier signal which contains actual information may remain small since the amplification ratio is constrained by the carrier signal which does not contain any actual information. This results in NFC device 102 achieving a limited sensitivity and poor signal to noise ratio (SNR).

In order to address the issue of poor SNR and limited sensitivity at the receiver of a NFC device, those skilled in the art have proposed of various carrier cancellation methods to remove the carrier signal from the signal received by the NFC device as much as possible so that the MI may be increased and the amplitude of the subcarrier signal after amplification would be much higher than the original.

In an approach proposed by one skilled in the art, a received load modulated signal is first sampled by an analogue to digital converter (ADC) and subsequently processed by a digital down converter (DDC) to generate I and Q branch signals. Then, a low-pass filter (LPF) is applied to each branch to obtain their corresponding direct-current (DC) components. The DC signals are then further sent to a pair of digital to analogue converters (DACs) and up converted using a pair of up-converters to generate the two branches of cancellation signals. The two branches of cancellation signals are then combined to produce a final cancellation signal that is used to cancel the carrier signal within the received load modulated signal.

However, the approach proposed above has three major shortcomings. First, although the method proposed ensures that the amplitude of the cancellation signal is close to that of the carrier signal, relatively high order LPFs are required to remove the non-DC components in the I and Q branches. The removal of the non-DC components are critical as any residual non-DC components could worsen the cancellation effect. Secondly, as the proposed method requires the use of a two-step analogue to digital and digital to analogue conversion process, it is almost inevitable that circuit delays will occur. When circuit delays occur, there is a strong likelihood that the phase of the cancellation signal may be

mismatched with the phase of the carrier signal. When this happens, the performance of the cancellation becomes unpredictable. Finally, as the proposed method requires the use of two additional DACs and two additional up-converters, this increases the overall cost of the proposed approach.

For the above reasons, those skilled in the art are constantly looking for a robust and low-cost carrier cancellation approach that may be used to improve the sensitivity of NFC devices when the devices are operating in reader mode. The approach should also address phase mismatches caused by circuit delays to ensure that the final performance of the cancellation is promising and repeatable.

Summary

The above and other problems are solved and an advance in the art is made by the apparatus and methods provided by embodiments in accordance with the invention.

A first advantage of the embodiments in accordance with the invention is that the effects of circuit delays are effectively negated by the use of logic control module which has been initialized based on a dual iterative system to select an optimal starting phase and optimum gain to be used to generate the cancellation signal.

A second advantage of the embodiments in accordance with the invention is that the invention is able to achieve a greatly improved Modulation Index metric for the subcarrier signal once the cancellation signal generated in accordance with the invention is applied to the received signal. This in turn reduces the quantization noise when the cancelled signal is sampled by an ADC thereby improving the signal to noise ratio.

A third advantage of embodiments in accordance with the invention is that the invention only requires the use of a single DAC and no up-converters thereby reducing the complexity and overall cost of the system.

A fourth advantage of the embodiments in accordance with the invention is that the invention is able to be easily implemented through software methods without significant modification to the existing original hardware.

According to a first aspect of the invention, a carrier cancellation system for generating an analogue cancellation signal, the system comprising: an analogue gain module configured to receive and amplify an analogue signal; an automatic gain control (AGC) module configured to: receive a digital signal, whereby the digital signal is converted

from the amplified analogue signal generated by the analogue gain module; adjust an analogue gain of the analogue gain module based on an estimated power level of the received digital signal to maintain the power level of the received digital signal at a predetermined optimal level; an initialized logic control module communicatively coupled to a system clock, the initialized logic control module being configured to: select an optimum gain entry from a gain look up table (LUT) and provide the selected gain entry to a multiplier; select a phase entry, once every clock cycle of the system's clock, from a phase LUT, beginning with the optimal starting phase entry and provide the selected phase entry to the multiplier, the multiplier being configured to multiply the selected optimum gain entry and the selected phase entry; and a DAC being configured to convert the multiplied signal generated by the multiplier to the analogue cancellation signal.

With regard to the first aspect of the invention, the initialization of the logic control module comprises the logic control module being configured to: initialize the logic control module when an analogue gain lock notification is received from the AGC module; select an initial starting phase entry from phase LUT and an initial gain entry from gain LUT, and provide the selected starting phase and gain entries to the multiplier to generate an initial cancellation signal; iteratively select a starting phase entry from the phase LUT until an optimal starting phase entry α_x is obtained, whereby the optimal starting phase entry α_x is defined as the starting phase entry that produces the lowest power of cancelled signal P_c , whereby P_c is defined as an estimated power of the received analogue signal after the received analogue signal has been cancelled by the cancellation signal; iteratively select a gain entry from the gain LUT until the optimum gain entry is selected, whereby the optimum gain entry is defined as a gain entry that produces the lowest power of cancelled signal P_c among all the gain entries in the gain LUT; and notify the AGC module to unlock and adjust an analogue gain of the analogue gain module based on a power level of the cancelled signal.

With regard to the first aspect of the invention the phase LUT comprises phase entries sampled from a sinusoidal wave cycle at a certain constant interval.

With regard to the first aspect of the invention, the system further comprises an optional post-DAC analogue gain module configured to amplify the analogue cancellation signal generated by the DAC.

With regard to the first aspect of the invention, the system further comprises an analogue-to-digital converter (ADC) configured to: convert the amplified analogue signal

generated by the analogue gain module into a digital signal; and provide the digital signal to the ADC module.

According to a second aspect of the invention, a method for generating an analogue cancellation signal using a carrier cancellation system comprising an analogue gain module, an automatic gain control (AGC) module, an initialized logic control module, a multiplier and a digital-to-analogue converter (DAC) is disclosed, the method comprising: receiving and amplifying, using the analogue gain module, an analogue signal; receiving, using the AGC module, a digital signal, whereby the digital signal is converted from the amplified analogue signal generated by the analogue gain module; adjusting, using the AGC module, an analogue gain of the analogue gain module based on an estimated power level of the received digital signal to maintain the power level of the received digital signal at a predetermined optimal level; selecting, using the initialized logic control module communicatively coupled to a system clock, an optimum gain entry from a gain look up table (LUT) and provide the selected gain entry to a multiplier; selecting, using the initialized logic control module, a phase entry, once every clock cycle of the system's clock, from a phase LUT, beginning with the optimal starting phase entry and providing the selected phase entry to the multiplier, multiplying, using the multiplier, the selected optimum gain entry and the selected phase entry; and converting, using the DAC, the multiplied signals generated by the multiplier to the analogue cancellation signal.

With regard to the second aspect of the invention, the step of initializing the logic control module comprises: initializing the logic control module when an analogue gain lock notification is received from the AGC module; selecting, using the logic control module, an initial starting phase entry from phase LUT and an initial gain entry from gain LUT, and providing the selected starting phase and gain entries to the multiplier to generate an initial cancellation signal; iteratively selecting, using the logic control module, a starting phase entry from the phase LUT until an optimal starting phase entry α_x is obtained, whereby the optimal starting phase entry α_x is defined as the starting phase entry that produces the lowest power of cancelled signal P_c , whereby P_c is defined as an estimated power of the received analogue signal after the received analogue signal has been cancelled by the cancellation signal; iteratively selecting, using the logic control module, a gain entry from the gain LUT until the optimum gain entry is selected, whereby the optimum gain entry is defined as a gain entry that produces the lowest power of cancelled signal P_c among all the gain entries in the gain LUT; and notifying, using the logic control module, the AGC module to unlock and adjust an analogue gain of the analogue gain module based on a power level of the cancelled signal.

With regard to the second aspect of the invention, the phase LUT comprises phase entries sampled from a sinusoidal wave cycle at a certain constant interval.

With regard to the second aspect of the invention, the method further comprises the step of: amplifying, using a post-DAC analogue gain module, the analogue cancellation signal generated by the DAC.

With regard to the second aspect of the invention, the method further comprises the step of: converting, using an analogue-to-digital converter (ADC), the amplified analogue signal generated by the analogue gain module into a digital signal, and providing the digital signal to the ADC module.

The above advantages are provided by embodiments of a device and method in accordance with the invention operating in the following manner.

Brief Description of the Drawings

The above advantages and features in accordance with this invention are described in the following detailed description and are shown in the following drawings:

Figure 1 illustrating a block diagram representative of a known NFC communication scenario whereby a NFC device is shown to be operating in reader mode and a NFC tag is shown to modulate a carrier signal transmitted from the NFC device;

Figure 2 illustrating plots showing the effects of amplitude and phase mismatches on the performance of cancellation;

Figure 3a illustrating a block diagram representative of components of a carrier cancellation system for generating an analogue cancellation signal in accordance with embodiments of the invention;

Figure 3b illustrating a plot showing a sinusoidal wave having multiple sampled points with a constant interval between each pair of sampled points in accordance with embodiments of the invention;

Figure 4 illustrating the amplitude of subcarrier signals in the frequency domain when a cancellation signal generated in accordance with embodiments of the invention is applied to a received load modulated signal and when the cancellation signal is not applied to the received load modulated signal; and

Figure 5 illustrating a block diagram representative of components in an electronic module for implementing embodiments in accordance with embodiments of the invention.

Detailed Description

This invention relates to a carrier cancellation system that is configured to generate a cancellation signal having an amplitude and phase that is almost equal to the amplitude and phase of a received carrier signal thereby effectively cancelling the carrier signal. This was achieved through the use of an initialized logic control module that was pre-initialized using a dual iterative approach to identify/search for an optimal starting phase entry and an optimum gain entry from two corresponding look up tables, whereby the selected phase and gain entries were used to generate a cancellation signal that had an amplitude and phase that closely matched the amplitude and phase of the received carrier signal.

One skilled in the art will recognize that some functional units in this description have been labelled as modules and/or components throughout the specification. The person skilled in the art will also recognize that a module may be implemented as circuits, logic chips or any sort of discrete component. Still further, one skilled in the art will also recognize that a module may be implemented in software which may then be executed by a variety of processor architectures. In embodiments of the invention, a module may also comprise computer instructions or executable code that may instruct a computer processor to carry out a sequence of events based on instructions received. The choice of the implementation of the modules is left as a design choice to a person skilled in the art and does not limit the scope of this invention in any way.

When a load modulated signal is cancelled by a cancellation signal, the resulting signal may be defined by the following equation:

$$\cos(2\pi f_c t + \alpha_c)[k_c + k_s \cos(2\pi f_s t + \alpha_s)] - k_x \cos(2\pi f_c t + \alpha_x) \quad \dots \text{Equation (1)}$$

where k_c is defined as the amplitude of the carrier signal, k_s is defined as the amplitude of the subcarrier signal, k_x is defined as the amplitude of the cancellation signal, f_c is defined as the frequency of carrier signal, f_s is defined as frequency of subcarrier signal, α_c is defined as the phase of the carrier signal, α_s is defined as the phase of the subcarrier signal, and α_x is defined as the phase of the cancellation signal.

When equation (1) is expanded and rearranged, the following equation is produced:

$$\left(\sqrt{1 - 2k_r \cos(\alpha_r) + k_r^2}\right) \sin\left\{2\pi f_c t + \tan^{-1}\left[\frac{1 - k_r \cos(\alpha_r)}{k_r \sin(\alpha_r)}\right]\right\} + k_s \cos(2\pi f_c t + \alpha_c) \cos(2\pi f_s t + \alpha_s) \quad \dots \text{Equation (2)}$$

where k_r is defined as the ratio of the amplitude of the cancellation signal to the amplitude of the carrier signal, $k_r = \frac{k_x}{k_c}$, and α_r is defined as the phase difference between the cancellation signal and the carrier signal, $\alpha_r = |\alpha_x - \alpha_c|$.

It should be noted that the first portion of equation (2) represents the residual carrier signal, and the second portion of equation (2) represents the load modulated subcarrier signal. From the above, it can be seen that in order to achieve high quality cancellation, the first portion is expected to be as small as possible. Hence, when the amplitude ratio k_r is equal to 1 and the phase difference α_r is equal to 0, the coefficient of the first portion, i.e. $\sqrt{1 - 2k_r \cos(\alpha_r) + k_r^2}$, becomes '0'.

In this ideal situation, the carrier signal would be perfectly cancelled by the cancellation signal. Hence, from the equations above, it can be seen that an ideal cancellation occurs when both the amplitude and phase of the cancellation signal equals to that of the carrier signal, i.e. zero amplitude mismatch and zero phase mismatch.

Figure 2 illustrates plots showing the effects of amplitude and phase mismatches on the cancellation performance. The x-axis of the plot in Figure 2 shows the phase mismatch between the cancellation signal and the carrier signal in degrees from -180 to 180. The y-axis of the plot in Figure 2 shows the power ratio of the cancelled signal to that of the original carrier signal in dB. It should be noted that a lower power ratio indicates higher cancellation performance. Plots 205, 210, 215 represent cancellation signals having various amplitude ratios (of the cancellation signal amplitude to that of the carrier signal amplitude). From these plots, it is shown that the power ratio spans symmetrically against phase mismatch, whereby the lowest power ratio of all the plots are achieved when the phase mismatch is equal to zero. It can also be seen that when the phase mismatch is at zero, and when the amplitude ratio is 100%, i.e. plot 210, the power ratio of the cancelled signal to that of the original carrier signal is at its lowest value. In conclusion, it can be said that the impact of amplitude mismatch and phase mismatch are independent of each other. It is also useful to note that when the amplitude ratio is 100%, i.e. plot 210, even a small phase mismatch can lead to large power ratio increments. Therefore, the phase mismatch caused by circuit delays is non-negligible and is actually quite significant.

Figure 3a illustrates carrier cancellation system 300 for generating an analogue cancellation signal in accordance with embodiments of the invention. As illustrated in Figure 3a, system 300 comprises signal combiner 306, analogue gain module 310, analogue-to-digital converter (ADC) 315, automatic gain control (AGC) module 320, logic control module 325, gain look-up-table (LUT) 330, phase LUT 335, multiplier 337, digital-to-analogue converter (DAC) 340 and optionally, post-DAC analogue gain module 345. The detailed workings of signal combiner 305, analogue gain modules 310 and 315, ADC 315, AGC module 320, multiplier 337 and DAC 340 are omitted for brevity as the operation of these components and/or modules are known to those skilled in the art.

In operation, system 300 first receives a carrier signal 305. The received signal 305 is then amplified by analogue gain module 310 before it is sampled and subsequently converted into digital signals by ADC 315. The digital signals are then provided to a digital signal processing (DSP) system 380 and to AGC module 320. It is useful to note that AGC module 320 is widely used in signal processing whereby its basic function is to estimate the power of a received signal and automatically adjust an analogue gain to maintain the received signal at a preferable level for processing. In embodiments of the invention, a power evaluation function inside AGC module 320 is leveraged to measure and/or estimate the power of received signal 305 based on the digital signals received from ADC 315 and based on its measurement, make the necessary adjustments to the gain produced by analogue gain module 310. AGC module 320 then provides the estimated power to initialized logic control module 325 which is communicatively connected to gain LUT 330 and phase LUT 335. Gain LUT 330 contains a set of values that correspond to a set of specific gains whereby the amplitude of a cancellation signal may be adjusted by selecting a different gain entry from gain LUT 330. As for phase LUT 335, it contains a set of phase values that are sampled from a sinusoidal wave at a certain constant interval. As an example, such a sinusoidal wave is illustrated in Figure 3b whereby this sinusoidal wave comprises 64 points with a constant interval of $360/64 = 5.625$ degrees. In embodiments of the invention, the interval may be determined by one skilled in the art.

Initialized logic control module 325 then analyses the power level of the received signal and selects /searches for an optimal starting phase entry from phase LUT 335 and an optimum gain entry from gain LUT 330. It is understood that the phase of the generated cancellation signal can be changed by changing the starting phase entry. The optimum gain entry and the optimal starting phase entry would have been identified by logic control module 325 when this module was initialized. Details of the initialization of logic control module 325 will be discussed in detail in the later sections.

Initialized logic control module 325 then provides the selected phase entry together with the selected gain entry to multiplier 337 to be multiplied. The multiplied signal is then provided to DAC 340. Initialized logic control module 325 circularly loops through the phase LUT beginning with the optimal starting phase entry, once every clock cycle of the system's clock, and provides the selected phase entry together with the selected gain entry to multiplier 337 to be multiplied until the system is turned off. The system's clock is designed such that a complete round of phase LUT looping would be equal to the period of the carrier signal, i.e. $1/f_c$.

DAC 340 then converts these multiplied signals into a sinusoidal analogue cancellation signal 350. Cancellation signal 350 is then combined with received signal 305 at combiner 306. In other embodiments of the invention, in the event that the maximum output power of DAC 340 is much lower than the power of received signal 305, cancellation signal 350 may be amplified by post-DAC analogue gain module 345 before this amplified cancellation signal is provided to combiner 306.

In accordance with embodiments of the invention, the initialization of logic control module 325 occurs as follows:

Step 1 (Launching): AGC module 320 first estimates the power of the carrier signal within received signal 305 and based on this estimated power, adjusts the gain of analogue gain module 310 accordingly. After the signal has been adjusted to an expected level, AGC module 320 shall then be locked thereby preventing the gain of analogue gain module 310 from being adjusted further. In embodiments of the invention, the estimated power of the carrier signal when AGC module 320 is locked is P_{full} .

During this launching step, an initial gain entry is selected from gain LUT 330 by logic control module 325 whereby this gain entry comprises a value that is close to the difference between P_{full} and the default output power of DAC output P_{DAC} . The main aim of choosing such a gain entry value is to ensure that the initial amplitude of the cancellation signal k_x is close to the amplitude of the carrier signal k_c . The initial phase of the cancellation signal α_x may be selected by logic control module 325, from the phase entries in phase LUT 335 randomly or according to an estimation of the phase of the cancellation signal α_c as estimated by other methods known to those skilled in the art. Logic control module 325 will then provide the selected gain entry and the selected phase entry to multiplier 337 so that the multiplier may generate an analogue cancellation signal according to the multiplication result. It should be noted that for every clock cycle of the system's clock, logic control module

325 circularly loops through the phase LUT beginning with the initial phase entry for DAC 340 to generate a sinusoidal-like cancellation signal with a frequency value equivalent to f_c .

Step 2 (Dual iterative scanning – phase): In embodiments of the invention, the dual iterative scanning process is conducted when received signal 305 comprises only carrier signals, i.e. before subcarrier signals are modulated onto the carrier signal.

Logic control module 325 will then scan/search through phase LUT 335 for an optimal starting phase entry α_x that produces the lowest power of cancelled signal P_c (defined as an estimated power of received signal 305 after it has been combined with cancellation signal 350).

This process is done by module 325 first selecting a new starting phase entry, and starting the circular looping process beginning from the newly selected starting phase entry. The power of a cancelled signal P_c is then estimated by AGC module 320. To recap, it is ideal for the power of the cancelled signal P_c to be low as it indicates that there is only a small phase mismatch between cancellation signal 350 and received signal 305.

A new starting phase entry is then iteratively selected from the phase LUT and the process above is repeated until an optimal starting phase entry α_x has been identified.

In summary, it can be said that a starting phase entry that provides the lowest power of the cancelled signal P_c throughout all the iterations is identified and recorded as the optimal starting phase entry α_x . In other embodiments of the invention, different starting phase entry selection strategies can be designed based on the variations of power ratios as shown in Figure 2 to accelerate the scanning process.

Step 3 (Dual iterative scanning – amplitude): In embodiments of the invention, logic control module 325 will iteratively select a gain entry from various gain values provided in gain LUT 330. Similar to the process in Step 2 above, for each iteration after the new gain selection has taken effect, the power of the cancelled signal P_c is estimated by AGC module 320. The gain entry selected from gain LUT 330 that provides the lowest power of the cancelled signal P_c throughout all the iterations is then recorded as the optimum gain entry. Once the optimum gain entry has been determined, logic control module 325 will then be initialized to use this gain value for all future processes. In embodiments of the invention, different gain selection strategies can be designed based on the variations of power ratios as illustrated in

Figure 2 to accelerate the scanning process.

As expected, the accuracies of the phase and gain scanning steps are highly dependent on the content of the two LUTs which may be varied as required by one skilled in the art without departing from the invention. In general, when larger LUTs having intervals with smaller step sizes are deployed, this will result in higher accuracies in selection of the gain and phase values.

Step 4 (Final amplification): After the cancellation signal has been generated based on the optimal phase and gain, AGC module 320 will be unlocked and it will be enabled to adjust the analogue gain of analogue gain module 310 so that the cancelled signal may be amplified to an expected level. As the majority of the carrier signal has been cancelled, the MI of the subcarrier signal would be increased thereby significantly improving the receiving sensitivity of system 300, the quantization noise of ADC module 315 would be reduced thereby significantly improving the signal to noise ratio (SNR) of system 300.

Simulation results

Figure 4 illustrates the simulated results of subcarrier signals received by a NFC device operating in reader mode when carrier cancellation signals (as generated in accordance with embodiments of the invention) are combined with the received load modulated signals, and when carrier cancellation signals are not applied to the received load modulated signals. In particular, plot 410 is a plot of subcarrier signals as received by a DSP of a NFC device when carrier cancellation signals are not provided while plot 405 shows a plot of subcarrier signals as received by a DSP of a NFC device when carrier cancellation signals are combined with the received load modulated signals. It can be seen that the power of the subcarrier signals for plot 405 is about 40 dB higher than the power of plot 410. This shows that the MI of the subcarrier signals are greatly improved when carrier cancellation signals generated by system 300 are applied to the received load modulated signal.

Figure 5 illustrates a block diagram representative of components that may be provided within an electronic device that may be in turn provided within any one of the modules or components illustrated in Figure 3a such as, but not limited to, logic control 325 or AGC module 320 for implementing embodiments in accordance with embodiments of the invention. One skilled in the art will recognize that the exact configuration of each electronic device provided within these modules or components may be different and the exact

configuration of electronic device 500 may vary and Figure 5 is provided by way of example only.

In embodiments of the invention, device 500 comprises controller 501 which is configured to be in data communication with other devices via a bus or data lines. Controller 501 includes memory 520, Central Processing Unit (CPU) 505 mounted on a circuit board that processes instructions and data for performing the method of this embodiment, an operating system 506, an input/output (I/O) interface 530 for facilitating communications with other devices through a communications interface.

Memory 520 and operating system 506 are in data communication with CPU 505 via bus 510. The memory components include both volatile and non-volatile memory and more than one of each type of memory, including Random Access Memory (RAM) 520, Read Only Memory (ROM) 525 and a mass storage device 545, the last comprising one or more solid-state drives (SSDs). One skilled in the art will recognize that the memory components described above comprise non-transitory computer-readable media and shall be taken to comprise all computer-readable media except for a transitory, propagating signal. Typically, the instructions are stored as program code in the memory components but can also be hardwired. Memory 520 may include a kernel and/or programming modules such as a software application that may be stored in either volatile or non-volatile memory.

Herein the term “CPU” is used to refer generically to any device or component that can process such instructions and may include: a microprocessor, microcontroller, programmable logic device or other computational device. That is, CPU 505 may be provided by any suitable logic circuitry for receiving inputs, processing them in accordance with instructions stored in memory and generating outputs (for example to the memory components or on display 540). In this embodiment, CPU 505 may be a single core or multi-core processor with memory addressable space. In one example, CPU 505 may be multi-core, comprising—for example—an 8 core CPU.

The above is a description of embodiments of a module and a method in accordance with the present invention as set forth in the following claims. Whilst certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes and equivalents will now occur to those of ordinary skill in the art. It is therefore to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

CLAIMS:

1. A carrier cancellation system for generating an analogue cancellation signal, the system comprising:
 - an analogue gain module configured to receive and amplify an analogue signal;
 - an automatic gain control (AGC) module configured to:
 - receive a digital signal, whereby the digital signal is converted from the amplified analogue signal generated by the analogue gain module;
 - adjust an analogue gain of the analogue gain module based on an estimated power level of the received digital signal to maintain the power level of the received digital signal at a predetermined optimal level;
 - an initialized logic control module communicatively coupled to a system clock, whereby initialization of the logic control module comprises the logic control module being configured to:
 - initialize the logic control module when an analogue gain lock notification is received from the AGC module;
 - select an initial starting phase entry from phase LUT and an initial gain entry from gain LUT, and provide the selected starting phase and gain entries to the multiplier to generate an initial cancellation signal;
 - iteratively select a starting phase entry from the phase LUT until an optimal starting phase entry α_x is obtained, whereby the optimal starting phase entry α_x is defined as the starting phase entry that produces the lowest power of cancelled signal P_c , whereby P_c is defined as an estimated power of the received analogue signal after the received analogue signal has been cancelled by the cancellation signal;
 - iteratively select a gain entry from the gain LUT until the optimum gain entry is selected, whereby the optimum gain entry is defined as a gain entry that produces the lowest power of cancelled signal P_c among all the gain entries in the gain LUT; and
 - notify the AGC module to unlock and adjust an analogue gain of the analogue gain module based on a power level of the cancelled signal,
 - the initialized logic control module being configured to:
 - select an optimum gain entry from a gain look up table (LUT) and provide the selected gain entry to a multiplier;
 - select a phase entry, once every clock cycle of the system's clock, from a phase LUT, beginning with the optimal starting phase entry and provide the selected phase entry to the multiplier,
 - the multiplier being configured to multiply the selected optimum gain entry and the selected phase entry; and

a digital-to-analogue converter (DAC) being configured to convert the multiplied signals generated by the multiplier to the analogue cancellation signal.

2. The carrier cancellation system according to claims 1 whereby the phase LUT comprises phase entries sampled from a sinusoidal wave cycle at a certain constant interval.
3. The carrier cancellation system according to claim 1 or 2, the system further comprising:
 - a post-DAC analogue gain module configured to amplify the analogue cancellation signal generated by the DAC.
4. The carrier cancellation system according to any one of claims 1 to 3, the system further comprising:
 - an analogue-to-digital converter (ADC) configured to:
 - convert the amplified analogue signal generated by the analogue gain module into a digital signal; and
 - provide the digital signal to the ADC module.
5. A method for generating an analogue cancellation signal using a carrier cancellation system comprising an analogue gain module, an automatic gain control (AGC) module, an initialized logic control module, a multiplier and a digital-to-analogue converter (DAC), whereby the step of initializing the logic control module comprises:
 - initializing the logic control module when an analogue gain lock notification is received from the AGC module;
 - selecting, using the logic control module, an initial starting phase entry from phase LUT and an initial gain entry from gain LUT, and providing the selected starting phase and gain entries to the multiplier to generate an initial cancellation signal;
 - iteratively selecting, using the logic control module, a starting phase entry from the phase LUT until an optimal starting phase entry α_x is obtained, whereby the optimal starting phase entry α_x is defined as the starting phase entry that produces the lowest power of cancelled signal P_c , whereby P_c is defined as an estimated power of the received analogue signal after the received analogue signal has been cancelled by the cancellation signal;
 - iteratively selecting, using the logic control module, a gain entry from the gain LUT until the optimum gain entry is selected, whereby the optimum gain entry is

defined as a gain entry that produces the lowest power of cancelled signal P_c among all the gain entries in the gain LUT; and

notifying, using the logic control module, the AGC module to unlock and adjust an analogue gain of the analogue gain module based on a power level of the cancelled signal,

the method comprising:

receiving and amplifying, using the analogue gain module, an analogue signal;

receiving, using the AGC module, a digital signal, whereby the digital signal is converted from the amplified analogue signal generated by the analogue gain module;

adjusting, using the AGC module, an analogue gain of the analogue gain module based on an estimated power level of the received digital signal to maintain the power level of the received digital signal at a predetermined optimal level;

selecting, using the initialized logic control module communicatively coupled to a system clock, an optimum gain entry from a gain look up table (LUT) and provide the selected gain entry to a multiplier;

selecting, using the initialized logic control module, a phase entry, once every clock cycle of the system's clock, from a phase LUT, beginning with the optimal starting phase entry and providing the selected phase entry to the multiplier;

multiplying, using the multiplier, the selected optimum gain entry and the selected phase entry; and

converting, using the DACm the multiplied signals generated by the multiplier to the analogue cancellation signal.

6. The method according to claim 5 whereby the phase LUT comprises phase entries sampled from a sinusoidal wave cycle at a certain constant interval.

7. The method according to claim 5 or 6, the method further comprising the step of:

amplifying, using a post-DAC analogue gain module, the analogue cancellation signal generated by the DAC.

8. The method according to any one of claims 5 to 7, the method further comprising the step of:

converting, using an analogue-to-digital converter (ADC), the amplified analogue signal generated by the analogue gain module into a digital signal, and providing the digital signal to the ADC module.