CLAIMS

1. A cell logic structure for a battery-indifferent or pure energy harvesting multi-mode system, the cell logic structure comprising:

a CMOS gate circuit;

a header circuit coupled to the CMOS gate circuit and comprising first and second header transistors for coupling in parallel between a supply voltage and the CMOS gate circuit; and

a footer circuit coupled to the CMOS gate circuit and comprising first and second footer transistors for coupling in parallel between the CMOS gate circuit and a ground voltage;

wherein the header and footer circuits are configured for switching between different operation modes of the multi-mode system, the different operation modes chosen from a range from a normal mode in which feedback paths from an output of the CMOS gate circuit to the gate of the second header transistor and to the gate of the second footer transistor are substantially or fully disabled for full swing in the output voltage of the CMOS gate circuit, and a leakage suppression mode in which the feedback paths are substantially or fully enabled.

2. The cell logic structure of claim 1, wherein the first and second header transistors comprise NMOS transistors.

3. The cell logic structure of claims 1 or 2, wherein the first and second footer transistors comprise PMOS transistors.

4. The cell logic structure of any one of claims 1 to 3, wherein the header and footer circuits are configured for disabling the feedback by overdriving the gates of the first header transistor and the first footer transistor.

5. A battery-indifferent or pure energy harvesting multi-mode system comprising:

an energy harvesting circuit for generating power for the multi-mode system;

one or more cell logic structures of any one of claims 1 to 4; and

a power management circuit for switching between the different operation modes of the multi-mode system.

6. The multi-mode system of claim 5, wherein the power management circuit comprises a self-startup circuit portion for gradually powering up the multi-mode system after an outage of power generated by the harvesting circuit.

7. The multi-mode system of claim 6, wherein the self-startup circuit portion is configured to sequentially power up partitions of the multi-mode system.

8. The multi-mode system of claim 7, wherein the self-startup circuit portion comprises a delay circuit for introducing a delay between power up of the respective partitions.

9. The multi-mode system of any one of claims 5 to 8, further comprising a battery configured to be recharged from the energy harvesting circuit, and, in one operation mode, power is provided to the multi-mode system at least partially by the battery, and in another operation mode, power is provided by the energy harvesting circuit only.

10. The multi-mode system of any one of claims 5 to 8, wherein in all operation modes of power is provided purely by different output levels of the energy harvesting circuit.

11. A method of operating a cell logic structure for a battery-indifferent or pure energy harvesting multi-mode system, the method comprising the steps of:

controlling a header circuit coupled to a CMOS gate circuit, the header circuit comprising first and second header transistors for coupling in parallel between a supply voltage and the CMOS gate circuit, and

controlling a footer circuit coupled to the CMOS gate circuit, the footer circuit comprising first and second footer transistors for coupling in parallel between the CMOS gate circuit and a ground voltage;

such that the multi-mode system is switchable between different operation modes, the different operation modes chosen from a range from a normal mode in which feedback paths from an output of the CMOS gate circuit to the gate of the second header transistor and to the gate of the second footer transistor are substantially or fully disabled for full swing in the output voltage of the CMOS gate circuit, and a leakage suppression mode in which the feedback paths are substantially or fully enabled.

12. The method of claim 11, wherein the first and second header transistors comprise NMOS transistors.

13. The method of claims 11 or 12, wherein the first and second footer transistors comprise PMOS transistors.

14. The method of any one of claims 11 to 13, comprising controlling the header and footer circuits for disabling the feedback by overdriving the gates of the first header transistor and the first footer transistor.

15. A method of operating a battery-indifferent or pure energy harvesting multi-mode system, comprising the steps of:

generating power for the multi-mode system using an energy harvesting circuit;

executing the method of any one of claims 11 to 14; and

switching between the different operation modes of the multi-mode system.

16. The method of claim 15, comprising gradually powering up the multi-mode system after an outage of power generated by the harvesting circuit.

17. The method of claim 16, comprising sequentially powering up partitions of the multi-mode system.

18. The method of claim 17, comprising introducing a delay between power up of the respective partitions.

19. The method of any one of claims 15 to 18, further comprising recharging a battery from the energy harvesting circuit, and, in one operation mode, power is provided to the multi-mode system at least partially by the battery, and in another operation mode, power is provided by the energy harvesting circuit only.

20. The method of any one of claims 15 to 18, wherein in all operation modes of power is provided purely by different output levels of the energy harvesting circuit.