What Is Claimed Is:

1. A chip structure, comprising:

a first lower chip structure; and

an upper chip structure on the first lower chip structure and having a pixel array region,

the first lower chip structure, comprising:

a first lower semiconductor substrate having a first side and a second side opposing each other;

a first portion on the first side of the first lower semiconductor substrate; and

a second portion on the second side of the first lower semiconductor substrate,

wherein the first portion of the first lower chip structure comprises a gate wiring,

the second portion of the first lower chip structure comprises a second side wiring and a heating element, and

the heating element is on a same plane as that of the second side wiring and has a length greater than that of the second side wiring.

2. The chip structure of claim 1, wherein the first lower chip structure comprises lower through electrodes electrically connected to the second side wiring and the heating element while passing through the first lower semiconductor substrate.

3. The chip structure of claim 1 or claim 2, wherein the second side wiring comprises a first surface having a first wiring contact region, and a second surface

having a second wiring contact region and opposing the first surface, and

the heating element comprises a first heating element side having a first heating element contact region and a second heating element contact region and a second heating element side opposing the first heating element side.

4. The chip structure of claim 3, further comprising:

a first heating element electrode electrically connected to the first heating element contact region;

a second heating element electrode electrically connected to the second heating element contact region;

a first wiring electrode electrically connected to the first wiring contact region; and

a second wiring electrode electrically connected to the second wiring contact region.

5. The chip structure of claim 4, wherein the first heating element electrode, the second heating element electrode, and the first wiring electrode are through electrodes passing through the first lower semiconductor substrate.

6. The chip structure of any one of claims 3 to 5, wherein a length between the first heating element contact region and the second heating element contact region is greater than a length between the first wiring contact region and the second wiring contact region.

7. The chip structure of any one of claims 3 to 6, wherein the first surface and

the first heating element side are substantially coplanar with each other.

8. The chip structure of any one of claims 1 to 7, wherein the first lower chip structure further comprises a temperature sensor.

9. The chip structure of claim 8, wherein the temperature sensor is on substantially the same plane as that of the second side wiring and the heating element.

10. The chip structure of any one of claims 1 to 9, further comprising a second lower chip structure, the first lower chip structure being between the upper chip structure and the second lower chip structure,

wherein the second lower chip structure, the first lower chip structure, and the upper chip structure are electrically connected to each other,

the second side wiring is electrically connected to the second lower chip structure, and

the heating element is insulated from the second lower chip structure.

11. A chip structure, comprising:

a lower chip structure, comprising:

a lower semiconductor substrate having a first side and a second side opposing each other;

a first portion on the first side of the lower semiconductor substrate, and having a gate wiring; and

a second portion on the second side of the lower semiconductor substrate, and having a second side wiring and a heating element,

wherein the heating element is on a same plane as that of the second side wiring and has a length greater than that of the second side wiring; and

the chip structure further comprising:

an upper chip structure disposed on the lower chip structure,

wherein the upper chip structure comprises photoelectric elements, color filters, and microlenses.

12. The chip structure of claim 11, wherein the first portion comprises a first wiring region and a second wiring region,

the second wiring region is a region in which an arrangement density of the gate wiring is higher than an arrangement density of the gate wiring in the first wiring region,

the second portion comprises a first heating region opposing the first wiring region and a second heating region opposing the second wiring region, and

the second heating region is a region in which an arrangement density of the heating element is lower than an arrangement density of the heating element in the first heating region.

13. The chip structure of claim 11, wherein the first portion is closer than the second portion to the upper chip structure.

14. The chip structure of any one of claims 11 to 13, further comprising an upper through electrode that extends into the first portion of the lower chip structure

while passing through the upper chip structure.

15. The chip structure of any one of claims 11 to 14, further comprising:

a first wiring electrode connected to a first wiring contact region of a first surface of the second side wiring;

a second wiring electrode connected to a second wiring contact region of a second surface of the second side wiring;

a first heating element electrode connected to a first heating element contact region of a first heating element side of the heating element; and

a second heating element electrode connected to a second heating element contact region of the first heating element side of the heating element,

wherein the second surface opposes the first surface,

the first surface is substantially coplanar with the first heating element side, and

the first wiring electrode, the first heating element electrode, and the second heating element electrode pass through the lower semiconductor substrate.

16. A chip structure, comprising:

a lower chip structure having a wiring and a heating element, the heating element being on a same plane as that of the wiring and having a length greater than that of the wiring; and

an upper chip structure disposed on the lower chip structure and having a pixel array region,

wherein the heating element overlaps a portion of the pixel array region, and

wherein an arrangement density of the wiring and an arrangement density of the heating element are configured to reduce temperature differences between different

areas of the pixel array region.

17. The chip structure of claim 16, wherein the heating element is configured to have a length for heating the portion of the pixel array region.

18. The chip structure of claim 16 or claim 17, further comprising:

a first wiring electrode connected to a first wiring contact region of the wiring;

a second wiring electrode connected to a second wiring contact region of the wiring;

a first heating element electrode connected to a first heating element contact region of the heating element; and

a second heating element electrode connected to a second heating element contact region of the heating element,

wherein the second wiring electrode is on a first plane and the first wiring electrode is on a second plane different than the first plane, and

the first wiring electrode, the first heating element electrode, and the second heating element electrode are substantially on the second plane.

19. The chip structure of any one of claims 16 to 18, wherein the lower chip structure further comprises a temperature sensor.