

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
 - a substrate including a cell array region and a through-silicon-via (TSV) region;
 - an insulation layer on the substrate within the cell array region and the TSV region, the insulation layer including a recess region within the TSV region;
 - a capacitor on the insulation layer within the cell array region;
 - a dummy support pattern on the insulation layer within the TSV region such that the dummy support pattern overlaps the recess region, when viewed in plan; and
 - a TSV electrode penetrating the dummy support pattern and the substrate.
2. The semiconductor device of claim 1, wherein the TSV electrode traverses the recess region.
3. The semiconductor device of claim 1, wherein an area of the dummy support pattern is greater than an area of the recess region, when viewed in plan.
4. The semiconductor device of claim 1, wherein the dummy support pattern comprises:
 - a first segment and a second segment, the first segment being at a center of the dummy support pattern, and the second segment being around the first segment such that the first segment is at a level lower than the second segment with respect to the substrate.
5. The semiconductor device of claim 4, wherein the second segment surrounds the first segment, when viewed in plan.

6. The semiconductor device of claim 4, wherein the first segment overlaps the recess region, when viewed in plan, and at least a portion of the second segment does not overlap the recess region, when viewed in plan.

7. The semiconductor device of claim 4, wherein the first segment and the second segment have substantially a same thickness.

8. The semiconductor device of claim 4, wherein the dummy support pattern further comprises:

a third segment connecting the first segment and the second segment.

9. The semiconductor device of claim 4, wherein the TSV electrode penetrates the first segment.

10. The semiconductor device of claim 1, further comprising:

a buried insulation pattern underneath the dummy support pattern with respect to the substrate such that the buried insulation pattern fills the recess region.

11. The semiconductor device of claim 10, wherein a sidewall of the buried insulation pattern is laterally recessed from a sidewall of the dummy support pattern.

12. The semiconductor device of claim 1, wherein the dummy support pattern is a first dummy support pattern, and the semiconductor device further comprises:

a second dummy support pattern between the insulation layer and the first dummy support pattern such that the TSV electrode penetrates the second dummy support pattern.

13. The semiconductor device of claim 12, wherein the second dummy support pattern comprises:

a first segment and a second segment, the first segment of the second dummy support pattern being at a center of the second dummy support pattern, and the second segment of the second dummy support pattern being around the first segment such that the first segment is at a level lower than that of the second segment with respect to the substrate.

14. The semiconductor device of claim 13, wherein
the first segment of the second dummy support pattern overlaps the recess region, when viewed in plan, and

at least a portion of the second segment of the second dummy support pattern does not overlap the recess region, when viewed in plan.

15. The semiconductor device of claim 1, further comprising:
a plurality of landing pads in the insulation layer within the cell array region, at least one of the plurality of landing pads being connected to the capacitor; and
a plurality of dummy pads in the insulation layer within the TSV region.

16. The semiconductor device of claim 15, wherein the plurality of dummy pads are not in the insulation layer within the recess region.

17. A semiconductor device, comprising:

a substrate including a cell array region and a through-silicon-via (TSV) region;

an insulation layer within the cell array region and the TSV region, the insulation layer including a recess region within the TSV region;

a plurality of bottom electrodes on the insulation layer within the cell array region;

a support pattern on sidewalls of the bottom electrodes;

a dummy support pattern on the insulation layer within the TSV region such that the dummy support pattern overlaps the recess region, when viewed in plan; and

a TSV electrode penetrating the dummy support pattern and the substrate.

18. The semiconductor device of claim 17, wherein a bottom surface of the dummy support pattern is at a level lower than a bottom surface of the support pattern with respect to the substrate.

19. The semiconductor device of claim 17, wherein a top surface of the dummy support pattern is substantially at a same level as a top surface of the support pattern with respect to the substrate.

20. A semiconductor device, comprising:

a substrate including a cell array region and a through-silicon-via (TSV) region;

an insulation layer on the substrate within the cell array region and the TSV region, the insulation layer including a plurality of recess regions within the TSV region;

a capacitor on the insulation layer within the cell array region;

a dummy support pattern on the insulation layer within the TSV region such

that the dummy support pattern overlaps the plurality of recess regions, when viewed in plan; and

a plurality of TSV electrodes penetrating the dummy support pattern and the substrate.