

VIDEO SIGNAL PROCESSOR

The present invention relates to video signal processors for converting digital RGB data into a composite video signal (NTSC system, for example) for displaying on CRT display unit through a digital-to-analog converter.

A prior art picture signal processor involves displaying a predetermined picture chromatically, for example, through outputting an analog signal indicating an amplitude value of each colour of R (red), G (green) and B (blue) to a special monitor set.

The operation of the picture signal processor comprises storing picture data in video RAM, reading the picture data out of the video RAM at every frame, addressing a colour data RAM having stored colour data of R, G, B with the picture data as address signal, subjecting the colour data read out of RAM to D/A conversion, thereby generating an analog RGB signal. The analog RGB signal is then output to the monitor set to display a colour picture.

When outputting a composite signal according to NTSC system, the operation is made on the colour data of R, G, B generated from the colour data RAM, a luminance signal and two colour difference signals are made out from the operation result, thus obtaining a composite video signal.

As another example, furthermore, digital RGB colour data is once converted into analog RGB signals through a D/A converter, the three signals are subjected to addition and subtraction analogically to generate a luminance signal (Y), a red colour difference signal (R - Y) and a blue colour difference signal (B - Y), thus obtaining a composite video signal.

However, according to the prior art video signal processor, because the luminance signal and the colour difference signals are obtained through operation on every picture element, there remain problems such that: the processor becomes inevitably large in size; power consumption is increased; conversion rate is low, and so forth.

Then, in the case of analogical processing, because the analog signal is of exceedingly high precision whichever system NTSC or PAL may work, it is difficult to handle a high composite signal.

An object of the invention is to provide an improved video signal processor and particularly, one for which miniaturisation in structure, a decrease in power consumption and an enhancement of conversion rate and precision are achieved.

Another object of the invention, is to provide a modulator adapted for construction as an MOS digital integrated circuit, so that a composite video signal may be generated with less harmonic component.

A further object of the invention is to provide a colour burst generator adapted for construction as an MOS digital integrated circuit, so that an accurate composite video signal can be generated.

A yet further object of the invention is to provide a digital-to-analog converter adapted for construction as an MOS digital integrated circuit, so that a composite video signal almost free from carrier leak and phase shift can be generated.

According to the present invention, there is provided a video signal processor provided with a colour pallet for converting a colour code for specifying a colour of each dot on a display picture into RGB colour data, and a conversion means for converting said RGB colour data converted as above into a luminance signal and two colour difference signals represented by analog values; said conversion means comprising a memory in which a conversion system for converting said RGB colour data represented by a digital value into said luminance signal and two colour difference signals represented by digital values, is stored; and a digital-to-analog converter for converting said digital value luminance signal and two colour difference signals into analog values.

Other features of importance to the invention reside in the balanced modulator disclosed, the colour burst generator disclosed and the digital-to-analog converter disclosed.

Further aspects of the invention may be found in the appended claims.

How the invention may be carried into effect is hereinafter particularly described with reference to the accompanying drawings, in which:-

Figure 1 is a block diagram showing a colour graphics display system in which the invention may be employed;

Figures 2 (a) and (b) are block diagrams showing a video signal generator including the invention;

Figure 3 is a block diagram showing a matrix ROM forming part of the generator of Figures 2 (a) and (b);

Figure 4 is a graph showing a vectorial result using the matrix ROM of Figure 3;

Figure 5 is a block diagram representing a first

example of a balanced modulator forming part of the generator of Figures 2 (a) and 2 (b);

Figures 6 (a) to (c) are waveform diagrams showing an operating state of the balanced modulator of Figure 5;

Figures 7 (a) to (d) are waveform diagrams showing an operating state of a video signal processor having the balanced modulator of Figure 5;

Figure 8 is a block diagram representing a second example of a balanced modulator;

Figures 9 (a) to (f) are waveform diagrams showing an operating state of the balanced modulator of Figure 8;

Figure 10 is a block diagram showing a colour burst signal generator forming part of the generator of Figures 2 (a) and 2 (b);

Figures 11 (a) to (c) are waveform diagrams showing an operating state of the colour burst signal generator of Figure 10;

Figure 12 is a block diagram showing a digital-to-analog converter forming part of the generator of Figures 2 (a) and 2 (b);

Figures 13 (a) to (e) are waveform diagrams showing an operating state of the converter of Figure 12; and

Figure 14 is a circuit diagram of a composite circuit forming part of the generator of Figures 2 (a) and 2 (b).

In the colour graphics display system shown in Figure 1, means for generating sound has been omitted, nor is it described herein. The system includes a CPU 101, a read only memory (ROM) 102 in which a control program is stored, a random access memory (RAM) 103 in which data, operational results and others are loaded

temporarily, and a video signal generator (VCE) 104 which receives picture data from a video display controller (VDC) 105, which picture of colour graphics display a background and a sprite that is in an animation moving on the background and is loaded in a video random access memory (VRAM) 106. The video signal generator 104 generates an analog RGB signal as output A and a composite signal as output B, which are fed to a TV receiver 109 through interfaces 107 and 108 respectively. The analog RGB signal is given directly to a cathode ray tube (CRT) of the receiver 109 as a special monitor, and the composite signal is given to the CRT by way of a receiving circuit. Thus, a picture according to the picture data can be displayed on the CRT of the TV receiver 109.

In one example (Figure 2(a)) of video signal generator 104, there are a data bus 221 for exchanging data with CPU 101 (Figure 1), another data bus 222 for exchanging data with the video display controller 105 (Figure 1), an address register 224 connected to the data bus 221, and an address selector 225 connected to the data bus 222. The address selector 225 selects one of data in the address register 224 or the data bus 222 as an address signal. The data bus 221 is also connected to a 512 x 9 bit colour table RAM or colour pallet 226 which receives address signals from the address selector 225. Colour data read from the colour pallet 226 at a time selected by a dot clock is latched in a data latch circuit 227. The primary colour data in the data latch circuit 227 are fed to red, green and blue digital-to-analog converters 228, 229 and 230 respectively, and to a 512 x 15 matrix ROM 231 having a signal conversion matrix for conversion into a luminance signal Y, and colour difference signals R - Y and B - Y.

A logic control unit 232 receives address signals A0 to A2, chip select signals $\overline{CS}$, write signal $\overline{WR}$, read signal $\overline{RD}$, output control signal CESEL and others from CPU 101 and its outputs control the address

- 5 register 224, the address selector 225, the colour pallet 226, the latch circuit 227, a synchronous logic control signal generator 233 and others (not shown). The control signal generator 233 has as input on line 255 a sine wave oscillation signal of 21.47727 MHz from
- 10 an oscillator 233A and has outputs horizontal synchronising signal $\overline{HSYNC}$, vertical synchronising signal $\overline{VSYNC}$, dot clock CK, sub-carriers of colour difference signals, modulation zero signals of colour difference signals, burst generating sub-carrier signal,
- 15 burst control signals and others. Both synchronising signals $\overline{HSYNC}$, $\overline{VSYNC}$ and dot clock CK are also fed to the video display controller 105. A synchronising signal composite circuit 234 compounds the horizontal and vertical synchronising signals on lines 251 and then
- 20 outputs a composite synchronising signal. Analog RGB signals from D/A converters 228, 229 and 230 and the composite synchronising signals from circuit 234 are input to an analog RGB signal output circuit 241A.

- The matrix ROM 231 has three output buses 258, 259
- 25 and 260, carrying the luminance Y signal, the colour difference R - Y signal and the colour difference B - Y signal, respectively. The colour difference signals R - Y and B - Y from the matrix ROM 231 are subjected to balanced modulation digitally in respective modulators
- 30 238 and 239 by the 0° and 90° sub-carriers of colour difference signals from control signal generator 233. The modulated signals R - Y and B - Y and the luminance signal Y are subjected to digital-to-analog conversion in D/A converters 236, 237 and 235 respectively. The

luminance signal Y on bus 258 has the synchronising signals on lines 251 superposed thereon by the D/A converter 235. Additionally, a burst circuit 240 receives as input from generator 233 a burst control signal on line 272 and a burst generating sub-carrier signal at 3.58 MHz on line 273, and its output to D/A converter 242 inserts eight to nine cycles in a back porch during a horizontal blanking period including the horizontal synchronising signal and outputs a burst signal. The burst control signal on line 272 becomes zero only during the time period for generating the burst signal and allows the sub-carrier signal on line 273 to pass to the D/A converter 242. The modified luminance signal Y, modulated colour difference signals R - Y and B - Y and the burst signal are output on lines 264, 265, 266 and 267 respectively in predetermined phase and timing and compounded to a composite video signal by a composite circuit 241B.

In the simple explanatory Figure 2 (b), the digital RGB colour data from the latch circuit 227 is provided in 3 bits, 1 bit each to respective inputs 252, 253 and 254 (Figure 2(b)) of the matrix ROM 231. In the matrix ROM 231, these are converted into digital composite video data constituted of 9 bits, 3 bits for Y signal, 3 bits for B - Y signal, and 3 bits for R - Y signal and supplied to respective output buses 258, 259 and 260. Thus eight colours can be represented according to combination of the three primary colours. The digital RGB data and the digital composite video data are co-ordinated with each other as shown in the following Table I.

TABLE I

Colour	RGB	Y		R - Y		B - Y	
	Binary number	Binary	Decimal	Binary	Decimal	Binary	Decimal
White	111	111	7	100	0	100	0
Yellow	110	110	6	101	1	000	-3
Cyan	011	101	5	000	-3	101	1
Green	010	100	4	001	-2	002	-2
Magenta	101	011	3	110	2	110	2
Red	100	010	2	111	3	010	-1
Blue	001	001	1	010	-1	110	3
Black	000	000	0	100	0	100	0

The binary number in Table I is data treated in the video signal processor according to the present invention, while the decimal number shows the analog value after D/A conversion. The analog value is represented as a decimal number so that the present invention may be readily understood.

The Y signal output on 258 of the digital composite video data is subjected to straight D/A conversion in D/A converter 235 to provide analog Y signal data on line 264 to circuit 241B. R - Y signal output on bus 259 and B - Y signal output on bus 260 are subjected to balanced modulation digitally through the digital balanced modulators 238 and 239 before D/A conversion in D/A converters 236 and 237 to provide analog R - Y data on line 265 and B - Y data on line 266 to circuit 241B. The burst signal from circuit 240 is subjected to D/A conversion in D/A converter 242 to give analog burst data on line 267 to circuit 241B.

In a practical example (Figure 3), the digital RGB colour data from data latch circuit 227 is provided in 9

bits or 3 bits each on respective inputs 303, 304 and 305, consisting of three lines 310 to the matrix ROM 231. In this way, 512 colours can be represented by different combinations of the three primary colours.

- 5 However, the digital composite video data output of the matrix ROM 231 on lines 311 is constituted of 15 bits, that is, 5 bits for Y signal, 5 bits for R - Y signal and 5 bits for B - Y signal.

10 The matrix ROM 231 is a semi-conductor memory in which data for 512 colours is stored beforehand. The following Table II sets out data stored in the semi-conductor memory for 50 typical colours of the 5122 colours available. The values are expressed in decimal form for simplicity's sake, though they are in fact in
15 binary form, as will be understood.

The conversion of RGB colour data into values for Y, R - Y and B - Y in the Table is described below. First, conversion into the luminance signal Y will be described. As is well known, the luminance signal Y is
20 obtained through Eq. (1).

$$Y = 0.3R + 0.59G + 0.11B \quad \dots (1)$$

$$0 \leq R \leq 1, 0 \leq G \leq 1, 0 \leq B \leq 1, 0 \leq Y \leq 1$$

25 To use within the range of $0 \leq Y' \leq 31$, $0 \leq R' \leq 7$, $0 \leq G' \leq 7$, the Eq. (1) is multiplied by 31/7 to convert into:

$$Y' = 1.33R' + 2.61G' + 0.49B' \quad \dots (1)'$$

30

Next, the colour difference signal R - Y will be obtained through:

$$\begin{aligned}
 R - Y &= R - (0.3R + 0.59G + 0.11B) \\
 &= 0.7R - 0.59G - 0.11B \quad \dots (2)
 \end{aligned}$$

$$\begin{aligned}
 0 \leq R \leq 1, \quad 0 \leq G \leq 1, \quad 0 \leq B \leq 1, \quad -0.7 \leq R - Y \\
 \leq 0.7
 \end{aligned}$$

5

To use within the range of $-15 \leq R' - Y' \leq 15$, $0 \leq R' \leq 7$, $0 \leq G' \leq 7$, $0 \leq B' \leq 7$, the Eq. (2) is multiplied by $15/(0.7 \times 7)$ to obtain:

$$R' - Y' = 2.14R' - 1.80G' - 0.34B' \quad \dots (2)'$$

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The colour difference signal $B - Y$ is then obtained through:

$$\begin{aligned}
 B - Y &= B - (0.3R + 0.59G + 0.11B) \\
 &= -0.3R - 0.59G + 0.89B \quad \dots (3)
 \end{aligned}$$

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$$\begin{aligned}
 0 \leq R \leq 1, \quad 0 \leq G \leq 1, \quad 0 \leq B \leq 1, \quad -0.89 \leq B - Y \\
 \leq 0.89
 \end{aligned}$$

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To use within the range of $-15 \leq B' - Y' \leq 15$, $0 \leq R' \leq 7$, $0 \leq G' \leq 7$, $0 \leq B' \leq 7$, the Eq. (3) is multiplied by $15/0.89 \times 7$ to obtain:

$$B' - Y' = -0.72R' - 1.42G' + 2.14B' \quad \dots (3)'$$

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30 Values of the luminance signal and the colour difference signals are obtained according to the Eqs. (1)', (2)' and (3)', and the values obtained through counting fractions over $1/2$ as one and dis-regarding the rest are given in the following Table II.

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TABLE II

RGB (Decimal)	Colour	Y (Decimal)	R - Y (Decimal)	B - Y (Decimal)
000	Black	0	0	0
001	Dark blue	0	0	2
002	gradual change ↓	1	-1	4
003		1	-1	6
004		2	-1	9
005		2	-2	11
006	Bright blue	3	-2	13
007	Blue	3	-2	15
100	Dark red	1	2	-1
200	gradual change ↓	3	4	-1
300		4	6	-2
400		5	9	-3
500		7	11	-4
600	Bright red	8	13	-4
700	Red	9	15	-5
101	Dark Magenta	2	2	1
202	gradual change ↓	4	4	3
303		5	5	4
404		7	7	6
505		9	9	7
606	Bright Magenta	11	11	9
707	Magenta	13	13	10
010	Dark Green	3	-2	-1
020	gradual change ↓	5	-4	-3
030		8	-5	-4
040		10	-7	-6
050		13	-9	-7
060	Bright green	16	-11	-9
070	Green	18	-13	-10
011	Dark cyan	3	-2	1
022	gradual change ↓	6	-4	1
033		9	-6	2
040		12	-9	3
055		16	-11	4
066	Bright cyan	19	-13	4
077	Cyan	22	-15	5
110	Dark yellow	4	0	-2
220	gradual change ↓	8	1	-4
330		12	1	-6
440		16	1	-9
550		20	2	-11
660	Bright yellow	24	2	-13
770	Yellow	28	2	-15
111	Dark gray	4	0	0
222	gradual change ↓	9	0	0
333		13	0	0
444		18	0	0
555		22	0	0
666	Bright gray	27	0	0
777	White	31	0	0

Figure 4 shows a so-called vectorial result obtained through converting the digital RGB colour data of the aforementioned 50 typical colours into digital composite video data. The abscissa shows B - Y signal, and the ordinate shows R - Y signal, as derived and plotted from the above Table. The different combinations of the values of each signal allow a variety of colouration.

The digital composite video data on output lines 311 are fed to fifteen flip-flops 302 (Figure 3) to adjust for any time lag between the data, which is latched in synchronism with dot clock 306 supplied from control signal generator 233 (Figure 2(a)). If the read time of the semi-conductor memory 231 is sufficiently shorter than one dot period of the data, then the flip-flops are not required. The outputs of the flip-flops 302 are grouped into three groups of five lines each for digital Y signal data 307, digital R - Y data 308 and digital B - Y data 309.

In the simple explanatory example of a modulator 238 or 239, shown in Figure 5, an output of 3 bits per signal from the matrix ROM 231 is assumed. The digital balanced modulator has three unmodulated data input terminals 530 receiving an output from ROM 231, a modulation clock input terminal 531 receiving an input from generator 233, three modulated data output terminals 532 which are connected to D/A converter 236 or 237, six inverters 533, six AND gates 534 and three OR gates 535. When the logic signal applied to the modulation clock input terminal 531 is 1, signals of the same logical value as the data inputs from the unmodulated data input terminals 530 are output to the output terminals 532. When the logic signal applied to the modulation clock input terminal 531 is 0, signals

inverse in logical value to the data input from unmodulated data input terminals 530 are output to the output terminals 532. The relations between R - Y data before modulation and R - Y data after modulation are shown in the following Table III.

TABLE III

10	Colour	R - Y before modulation		R - Y after modulation			
				Modulation clock = 1		Modulation clock = 0	
		Binary	Decimal	Binary	Decimal	Binary	Decimal
	White	100	0	100	0	011	0
	Yellow	101	1	101	1	010	-1
15	Cyan	000	-3	000	-3	111	3
	Green	001	-2	001	-2	110	2
	Magenta	110	2	110	2	001	-2
	Red	111	3	111	3	000	-3
	Blue	010	-1	010	-1	101	1
20	Black	100	0	100	0	011	0

Although data are represented as decimal numbers in the above Table III, the data are actually handled as binary numbers.

Figure 7 is a waveform diagram showing the operating condition of the circuit of Figure 5. When the R - Y clock of Figure 7 (a) is input to terminal 531 of Figure 5, the normal logical value and inverse logical value, which are output from terminals 530, are output as shown in Figure 7 (b). The B - Y clock of Figure 7 (c) is phase displaced by 90° from that of Figure 7 (a) and the B - Y output is as shown in Figure

7 (d). Thus, when the clock signals applied to terminal 531 of Figure 5 are as in Figure 6 (a) and the data (represented decimally) applied to terminals 530 are as in Figure 6 (b), the output at terminals 532

5 (represented decimally) are as in Figure 6 (c). It will be appreciated that the data are actually handled as binary numbers.

10 A sub-carrier of colour difference signal (3.58 MHz in NTSC system, or 4.43 MHz in PAL system) is input to the modulation clock input terminal 531, thereby obtaining a colour difference signal output in balanced modulation.

15 Two sub-carriers of colour difference signals shifted 90° in phase will be obtainable, for example, by providing a clock signal at twice the frequency of the sub-carrier of colour difference signal and then dividing it. By using one as the modulation clock of the R - Y signal and the other as the modulation clock of the B - Y signal, modulation outputs of the R - Y
20 signal and B - Y signal are obtainable as shown in Figure 6 (c).

In another practical example (Figure 8), of a modulator 238 or 239, a 5 bit input R - Y or B - Y signal is used as in Figure 3. The R - Y or B - Y
25 signals on lines 308 or 309 from ROM 231 are connected to unmodulated data input terminals 830 to 834, representing bits of decreasing significance. Each input terminal is connected through inverter, AND gates and an OR gate (similar to those of Figure 5) to an
30 output. That of terminal 830 is taken to an OR gate 842 and those of terminals 831 to 834 to respective AND gates 843. These gates are connected to output terminals 835 to 839.

The modulated data output terminals 835 to 839 are

connected to the D/A converter 236, and represent bits of decreasing significance. A modulation clock input terminal 840 is connected either to line 270 or to line 271 to receive a sub-carrier of colour difference signal from generator 233 and is connected directly and through inverters to the AND gates of the input terminal circuits as in Figure 5. An input terminal 841 connected to OR gate 842 and through inverter 844 to AND gates 843 receives a modulation zero signal from generator 233. This output from generator 233 is not shown in Figure 2.

When the logic signal of the modulation clock at terminal 840 is 1, a signal of the same logical value as the input signal at terminals 830 to 834 is output to the output terminals 835 to 839. When the logic signal of the modulation clock is 0, a signal inverse in logical value to the input signal is output to the output terminals. In addition, when the logic signal of the modulation zero signal input is 1, the signal at output terminal 835 is logic 1 and at terminals 836 to 839 is logic 0, regardless of the input states. The outputs on terminals 835 to 839 are input to a D/A converter 236 or 237 (Figure 2 (a)).

The following Table IV shows the relation between a colour difference signal before modulation which is input to the balanced modulator of the invention, a sub-carrier of colour difference signal working as the modulation clock, a modulation zero signal generated at a phase shift point of the colour difference sub-carrier, and analog values after subjecting colour difference signals in balanced modulation according to the above signals to D/A conversion in the D/A converter.

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Accordingly, when logic of the modulation zero input is 1, the analog value output by the D/A converter is to be zero. Table IV indicates the case where amplified on the D/A converter output varies between -

5 1.5V and 1.5V. The D/A conversion output when logic of the modulation zero input is 1 is defined generally as half the difference between the maximum output level and the minimum output level, namely the mid-point of D/A conversion outputs. A multiple of the frequency of sub-

10 carrier of colour difference signal, for example, a sextuple, is applied to a clock input terminal 255 in Figure 2(a) which is supplied oscillation signal of 21.47727 MHz from the oscillator 233A and pulses of Figures 9 (a), 9 (b), 9 (d) and 9 (e) of about 3.58 MHz

15 are generated by division in the control signal generator 233. The R - Y and B - Y colour difference signals from the matrix ROM 231, are subjected to balanced modulation by R - Y modulation clock signal pulse (Figure 9 (a)), the R - Y modulation zero signal

20 pulse (Figure 9 (b)), the B - Y modulation clock signal pulse (Figure 9 (d)) and the B - Y modulation zero signal pulse (Figure 9 (e)). These modulated signals are subjected to D/A converter, thereby obtaining R - Y analog output (Figure 9 (c)) and B - Y analog output

25 (Figure 9 (f)). By this means, the balanced modulator is capable of outputting a ternary value, positive, zero or mid-point, and negative. As will be apparent from Figure 9, the R - Y modulation clock signals and B - Y modulation clock signals are colour difference signal

30 sub-carriers phase shifted 90° apart. The modulation zero signal is generated when the corresponding sub-carrier phase changes and then it changes the output of the colour difference signal generated by the D/A converter to the mid-point between high and low levels.

The modulation zero signals are phase shifted 180° apart.

Examples of the burst circuit 240 and the burst D/A converter 242 of Figure 2 will be described next.

5 Figure 10 represents a practical example of a burst circuit 240 and a burst D/A converter 242 (Figures 2 (a) and 2 (b)).

10 The burst circuit has two input terminals, a burst control signal terminal 1030, and a sub-carrier signal terminal 1031. A burst control signal (272 in Figure 2(a) and 2(b), and Figure 11 (a)) in which logic becomes zero only during the time period for generating a burst signal is applied to terminal 1030 and a burst generating sub-carrier signal (273 in Figure 2(a) and 15 2(b) and Figure 11 (b)) is applied to the terminal 1031. The terminal 1030 is connected directly to two NOR gates 1038 and through an inverter 1037 to a third NOR gate 1038. The terminal 1031 is connected through one inverter 1037 to one of the two NOR gates 1038 and 20 through two inverters 1037 to the second of the two NOR gates 1038. The outputs of the NOR gates are taken to respective transmission gates, each comprising a pair of MOSFETs. The transmission gate associated with the one NOR gate consists of a P-channel MOSFET 1040 and an N-channel MOSFET 1041. The transmission gate associated with the third NOR gate consists of a P-channel MOSFET 1042 and an N-channel MOSFET 1043, whilst the transmission gate associated with the second NOR gate consists of a P-channel MOSFET 1044 and an N-channel 25 MOSFET 1045. The outputs of the NOR gates are taken directly to the N-channel sides of the transmission gates and through inverters 1037 to the P-channel sides. The output sides of the transmission gates are commoned to an output terminal 1033 and balanced by equal 30

resistance resistors 1035 and 1036 to high and low value terminals 1032 and 1033. The analog burst data signal (Figure 11 (c)) is thus generated, and is shown in Table V.

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TABLE V

Burst control (1030)	Subcarrier (1031)	Q ₁ (1040)	Q ₂ (1041)	Q ₃ (1042)	Q ₄ (1043)	Q ₅ (1044)	Q ₆ (1045)	Output voltage (1033)
0	0	OFF		OFF		ON		Low level (1034)
0	1	ON		OFF		OFF		High level (1032)
1	0	OFF		ON		OFF		Mid-point level
1	1	OFF		ON		OFF		Mid-point level

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A practical example of a digital-to-analog converter 236 or 237 is represented in Figure 12. A blanking signal for showing the display term is input to terminal 1230. When the blanking signal is 1, the

20 display term is OFF. The same modulation zero signal as is input to terminal 841 (Figure 8) is input to terminal 1231. When the modulation zero signal is 1, the phase sub-carrier of colour difference signal is changed.

25 The modulated colour difference signals output from terminals 835 to 839 (Figure 8) are input to terminals 1232 to 1236 respectively, and applied directly to five buses and through inverters 1243 to five other buses.

The signals on the buses are de-coded by NAND gates 1241 connected to different combinations of buses. Accord-

30 dingly, only one NAND gate 1241 outputs zero to an associated NOR gate 1242. A NOR gate 1247 fed from terminals 1230 and 1231 outputs zero when the display term is OFF and sub-carrier of colour difference signal is changed. The NOR gates 1242 receives this output

through an inverter 1243, thereby entirely outputting zero. This output is also taken through an inverter 1243 and directly to MOSFETs 1245 and 1246 of a transmission gate connected to an output terminal 1238.

5 Each NOR gate 1242 is also connected to a transmission gate consisting of MOSFETs 1245 and 1246, through an inverter 1243 and directly. The transmission gates are connected by equal resistance dividing resistors 1244, so that when ON, the output of terminal 1238 is the
10 centre level. When the output of NOR gate 1247 is 1, one of the NOR gates 1242 which inputs the output of decoder outputs 1, the analog output according to the logic of terminals 1232 to 1236 is obtained at terminal 1238. Digital data before and after balanced modulation
15 are shown in the following Table VI.

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TABLE VI

Digital value before modulation		Digital value after modulation			
		Modulation clock=1		Modulation clock=0	
Binary	Decimal	Binary	Decimal	Binary	Decimal
11111	+15	11111	+15	00000	-15
11110	+14	11110	+14	00001	-14
11101	+13	11101	+13	00010	-13
11100	+12	11100	+12	00011	-12
11011	+11	11011	+11	00100	-11
11010	+10	11010	+10	00101	-10
11001	+ 9	11001	+ 9	00110	- 9
11000	+ 8	11000	+ 8	00111	- 8
10111	+ 7	10111	+ 7	01000	- 7
10110	+ 6	10110	+ 6	01001	- 6
10101	+ 5	10101	+ 5	01010	- 5
10100	+ 4	10100	+ 4	01011	- 4
10011	+ 3	10011	+ 3	01100	- 3
10010	+ 2	10010	+ 2	01101	- 2
10001	+ 1	10001	+ 1	01110	- 1
10000	0	10000	0	01111	0
01111	0	01111	0	10000	0
01110	- 1	01110	- 1	10001	+ 1
01101	- 2	01101	- 2	10010	+ 2
01100	- 3	01100	- 3	10011	+ 3
01011	- 4	01011	- 4	10100	+ 4
01010	- 5	01010	- 5	10101	+ 5
01001	- 6	01001	- 6	10110	+ 6
01000	- 7	01000	- 7	10111	+ 7
00111	- 8	00111	- 8	11000	+ 8
00110	- 9	00110	- 9	11001	+ 9
00101	-10	00101	-10	11010	+10
00100	-11	00100	-11	11011	+11
00011	-12	00011	-12	11100	+12
00010	-13	00010	-13	11101	+13
00001	-14	00001	-14	11110	+14
00000	-15	00000	-15	11111	+15

When a blanking signal (Figure 13 (a)) is logic 1 and a modulation zero signal (Figure 13 (b)) is logic 1, the D/A converter outputs a mid-point between high level output at terminal 1237 and low level output at terminal 1239. Otherwise, one transmission gate consisting of P-channel MOSFET 1245 and N-channel MOSFET 1246, as determined according to values of digital data after balanced modulation at terminals 1232 to 1236, becomes conductive, and the corresponding level is output at terminal 1238. When there is no colour difference component present (or at the time of achromatic colour such as black or the like), the digital data before balanced modulation is 10000 or 01111 (binary). The data becomes 10000 (binary) and 01111 (binary) through balanced modulation, however, the mid-point between high level and low level is output by the D/A converter because there are no balancing resistors 1244 between the corresponding transmission gates.

With unmodulated digital data input as in Figure 13 (c), the output is shown after modulation in Figure 13 (d), and after D/A conversion, the analog signal output is shown in Figure 13 (e). The phase of the analog signal output is determined by the phase of the modulation zero signal input (Figure 13 (b)) and is not related to an amplitude of the digital data. Further, because switching for balanced modulation is carried out always in a modulation zero state, incorrect data will never be output transiently.

Moreover, when the modulation zero signal is logic 1, the outputs of terminals 835 to 839 (Figure 8) are 10000 and are input to terminals 1232 to 1236 (Figure 12) so that D/A converter outputs a mid-point between high level and low level. Accordingly, terminal 1231 may be unnecessary in Figure 12 because D/A converter

outputs a mid-level at changing the phase of sub-carrier of colour difference signal by reason of the outputs of Figure 8. Alternatively, OR gate 842 and AND gates 843 in Figure 8 may be unnecessary if there is the terminal 5 1231 in Figure 12.

A practical example of the composite circuit 241B of Figure 2 is shown in Figure 14. A digital Y signal, a modulated digital R - Y signal, a modulated digital B - Y signal and a digital colour burst signal are each 10 converted into analog signals in respective digital-to-analog converters 235, 236, 237 and 242. The analog signals are input to terminals 1431, 1432, 1433 and 1434 of the composite circuit 241B, and a composite video signal is output. The input analog signals corresponding to the Y signal, R - Y signal, B - Y signal and 15 colour burst signal are input to individual resistors 1436 connected to the base of a transistor 1438. The collector of the transistor 1438 is connected to a power supply voltage +VCC and the emitter to one side of a 20 capacitor 1437 whose other side is an output terminal 1435, and through a resistor 1436 to a voltage -VEE. Thus, a composite video signal is output to the terminal 1435.

If the Y signal, R - Y signal, B - Y signal and 25 colour burst signal are compounded in a circuit as shown in Figure 14, and the resistance value of each resistor 1436 is adjustable, the phase and amplitude of each signal can be adjusted independently, thereby realising adjustment and correction of a tint.

30 As described above, according to the invention, digital RGB colour data can be converted straight into digital composite video data without conversion into an analog signal, so that conversion of high stability and precision may be achieved. Further, the replacement of

prior art D/A converter, analog adder-subtractor and A/D converter by a semi-conductor memory enables miniaturation, low power consumption and high speed operation of the processor to be achieved.

5 Composite video data different in hue to the same RGB colour data is obtainable by modifying the stored contents of the semi-conductor memory, to achieve another effect such that data may be adjusted independently for every indicateable colour or further
10 also independently for Y signal, R - Y signal and B - Y signal.

By the first example of modulator forming part of the invention, two colour difference signals can be subjected to balanced modulation through a digital
15 circuit, so that the video signal processor is capable of generating a composite video signal precise both in amplitude and phase angle such as has never been obtainable hitherto.

By a second example of modulator, data is
20 subjected digitally to balanced modulation so that the analog conversion of the modulated data will be a ternary value coming in positive value, mid-point and negative value, and thus the output comes near to a sine wave. Thus, the video signal processor is capable of
25 generating a composite video signal with less harmonic component than hitherto.

By means of a colour burst signal generator forming part of the invention, a high level (maximum value) and a low level (minimum value) of the colour
30 burst signal are generated alternately by MOS digital circuit, and an intermediate level is output when the colour burst signal is not generated. Thus, the video signal processor can generate a composite video signal superior both in amplitude characteristic and phase

characteristic.

In a digital-to-analog converter forming part of the invention, the output level becomes constant in value when there is blanking or no colour difference component present, so that a carrier leak will never arise. The phase does not shift, regardless of the magnitude of the amplitude, and a phenomenon or glitch by which incorrect data is output transiently never results, thus ensuring a composite video signal of an accuracy which has never been obtainable hitherto.

By the use of a composite circuit forming part of the invention, a luminance signal, two colour difference signals and a colour burst signal are compounded by adjustable means such as a resistor or the like to a composite video signal, thereby allowing adjustment or correction of a tint which is effective to achieve correct colour information.

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CLAIMS

1. A video signal processor provided with a colour
pallet for converting a colour code for specifying a
5 colour of each dot on a display picture into RGB colour
data, and a conversion means for converting said RGB
colour data converted as above into a luminance signal
and two colour difference signals represented by analog
values; said conversion means comprising a memory in
10 which a conversion system for converting said RGB colour
data represented by a digital value into said luminance
signal and two colour difference signals represented by
digital values, is stored; and a digital-to-analog
converter for converting said digital value luminance
15 signal and two colour difference signals into analog
values.
2. A processor as claimed in claim 1 comprising means
for latching each conversion output of said memory
according to the same clock signal.
- 20 3. A processor as claimed in claim 1 or 2, comprising
a balanced modulator for modulating said digital value
two colour difference signals digitally according to two
sub-carriers of colour difference signals represented by
digital values and 90° different in phase to each other.
- 25 4. A processor as claimed in claim 3, in which the
balanced modulator comprises a first logic circuit for
multiplying logically said colour difference signal and
said sub-carrier of colour difference signals, a second
logic circuit for multiplying the logically inverted
30 signal of said colour difference signal and the inverted
signal of said sub-carriers of colour difference
signals, and a third logic circuit for adding logically
each output of said first and second logic circuits and
out-putting said modulated colour difference signal.



5. A processor as claimed in claim 1 or 2, comprising a balanced modulator for modulating said digital colour difference signals according to digital colour difference signal sub-carriers and supplying a digital-to-analog converter with such modulated signals, the balanced modulator controlling the converter to a mid-point level of the analog output range when the phase of the sub-carrier of colour difference signal changes.
6. A processor as claimed in claim 5, wherein said balanced modulator includes a plurality of first logic circuits for multiplying logically each bit value of said colour difference signals and value of said colour difference signal sub-carrier, a plurality of second logic circuits for multiplying logically an inverted value of each bit value of said colour difference signals and an inverted value of said colour difference signal sub-carrier, a plurality of third logic circuits for adding logically outputs of said first and second logic circuits corresponding to each bit of said colour difference signals, and a fourth logic circuit group effective when input with outputs of said third logic circuits and a clock signal generated at the phase change point of said colour difference signal sub-carrier, so as to output a mid-point level of the analog output range when the phase of said sub-carrier of colour difference signal changes.
7. A processor as claimed in any preceding claim, wherein said digital-to-analog converter for converting said digital colour difference signals into analog values, is effective to output a mean value of the maximum output level and the minimum output level of said analog values during a period of time other than that for display and when said colour difference signals are none, and to output an analog value corresponding to



said colour difference signals between said maximum output level and minimum output level during a period of time when said colour difference signals within the display period are present.

- 5 8. A processor as claimed in claim 7, wherein said digital-to-analog converter has a first terminal for providing the maximum output level of said analog value, a second terminal for providing the minimum output level of said analog value, a plurality of resistors
10 connected in series between said first and second terminals and forming nodes between the resistors and between the resistors and terminals, an output terminal of said analog value, MOS transistor transmission gates connected between each node and said output terminal and
15 selectively operable to conduct according to said colour difference signals, and an additional MOS transistor transmission gate inserted between the mean point of the nodes and said output terminal and operable to conduct during a period of time other than that for display and
20 when said colour difference signals are none.

9. A processor as claimed in any preceding claim, including a colour burst signal generator for outputting maximum value and minimum value of a colour burst signal alternately according to the frequency of a sub-carrier
25 of colour burst signal during a period of time for generating the colour burst signal, outputting a value intermediate the maximum value and minimum value of said colour burst signal, during a period of time other than that for generating the colour burst signal.

- 30 10. A processor as claimed in claim 9, said colour burst signal generator comprising a first terminal for providing maximum value of said colour burst signal, a second terminal for providing minimum value of said colour burst signal, two resistors connected in series



between said first and second terminals, and MOS transistor transmission gates connected between nodes formed between resistors and between resistors and terminals, and an output terminal of said colour burst signal.

11. A processor as claimed in claim 1, in which said digital-to-analog converter comprises a first digital-to-analog converter for said luminance signal, and second and third digital-to-analog converters for said two colour difference signals, and which includes a colour burst signal generator for outputting a colour burst signal, each output terminal of said first, second and third digital-to-analog converters and of said colour burst signal generator is connected in the common to a bi-polar transistor through a resistor or the like, whereby each output level can be adjusted individually, and a composite video signal formed by compounding each signal is output from said bi-polar transistor.

12. A video signal processor substantially as hereinbefore described with reference to the accompanying drawings.
