NANO-SENSE AMPLIFIER FOR MEMORY

DESCRIPTIVE ABSTRACT

The invention, according to a first aspect, relates to a sense amplifier for a series of cells of a memory, including:

- a writing stage comprising a CMOS inverter, the input of which is directly or indirectly connected to an input terminal of the sense amplifier, and the output of which is connected to an output terminal of the sense amplifier intended to be connected to a local bitline addressing the cells of said series,

- a reading stage comprising a sense transistor, the gate of which is connected to the output of the inverter and the drain of which is connected to the input of the inverter.

FIG. 2