

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a substrate having a memory cell region, a peripheral region, and a dam region between the memory cell region and the peripheral region, the memory cell region having a rectangular shape according to a top view and having a plurality of active regions defined therein; a plurality of bit line structures extending on the substrate in the memory cell region to be parallel with each other in a first horizontal direction, each including a bit line; a plurality of buried contacts filling lower portions of spaces among the plurality of bit line structures on the substrate; a plurality of landing pads on the plurality of buried contacts; and a dam structure including a first dam structure and a second dam structure in the dam region and being at the same level as the plurality of landing pads.

FIG. 4