transistor 303 of Fig. 1 is reported on Fig. 2b. The result is that the total size is of the order of $6W_{303}$. Thus, the circuit of Figs. 2a and 2b proves to be actually simpler than that of Fig. 1, nevertheless it remains area consuming.

## SHORT DESCRIPTION OF THE INVENTION

Embodiments of the invention seek to provide a circuit which does not have the drawbacks mentioned earlier, in particular a relatively not very bulky, low consumption circuit, which may be used as a wordline driver circuit in a memory array.

Embodiments of the invention also seek to provide a particularly simple and not very bulky circuit which may be used for providing different logic functions.

According to a first aspect~~,~~ of the present invention, there is provided a circuit including a transistor of ~~a first~~ P-type ~~of~~ channel in series with a transistor of ~~a second~~ N-type ~~of~~ channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates~~,~~ said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential, ~~characterized in that~~wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate~~,~~ wherein said circuit provides the logic NOR function, and wherein the second control gates are biased by a same second gate signal and the first terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, whereas the second terminal for application of a power supply potential is biased at an OFF state.

According to a second aspect of the present invention, there is provided a circuit including a transistor of a P-type channel in series with a transistor of a N-type channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential, wherein said circuit provides the logic NAND function, and wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate, wherein the

second control gates are biased by a same second gate signal and wherein the second terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, the first terminal for application of a power supply potential is biased to a ON state.

Certain preferred but non-limiting embodiments of this device are the following:

~~- the second control gates are biased by a same second gate signal and the first or the second terminal for application of a power supply potential is biased by the complementary signal of said second gate signal;~~

~~- when the first terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, the second terminal for application of a power supply potential is biased at a OFF state;~~

- the transistor of the second type of channel is configured in order to operate in a depletion mode when the second gate signal is in the ON state;

## CLAIMS

1. A circuit including a transistor of ~~a first~~ P-type ~~of~~ channel in series with a transistor of ~~a second~~ N-type ~~of~~ channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first ~~($G_{1P}$, $G_{1N}$)~~ and a ~~($G_{2P}$, $G_{2N}$)~~ second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential,

~~characterized in that~~ wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate ~~($G_{2P}$, $G_{2N}$)~~,

wherein said circuit provides the logic NOR function, and

wherein the second control gates are biased by a same second gate signal and the first terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, whereas the second terminal for application of a power supply potential is biased at an OFF state.

~~2. The circuit according to claim 1, wherein the second control gates are biased by a same second gate signal and the first or the second terminal for application of a power supply potential is biased by the complementary signal of said second gate signal.~~

~~3. The circuit according to claim 2, wherein when the first terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, the second terminal for application of a power supply potential is biased at a OFF state.~~

42. The circuit according to claim ~~3~~1, wherein the transistor of the ~~second~~ N-type of channel is configured in order to operate in a depletion mode when the second gate signal is in the ON state.

~~53~~. ~~The circuit according to claim 2,~~ A circuit including a transistor of a P-type channel in series with a transistor of a N-type channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential, wherein said circuit provides the logic NAND function, and wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate, wherein the second control gates are biased by a same second gate signal and wherein ~~when~~ the second terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, the first terminal for application of a power supply potential is biased to a ON state.

~~64~~. The circuit according to claim ~~53~~, wherein the transistor of the ~~first~~ P-type of channel is configured in order to operate in a depletion mode when the second gate signal is in the OFF state.

~~7. The circuit according to claim 1, wherein the first terminal for application of a power supply potential is biased at a ON state, whereas the second terminal for application of a power supply potential is biased at a OFF state.~~

~~8.~~5. The circuit according to any of the preceding claims, including an input node connected to the first control gate of each of the transistors and an output node connected to the middle point of the serial association of the transistors.

~~9.~~6. The circuit according to any of the preceding claims, wherein the transistors are fully depleted.

~~10.~~7. The circuit according to any one of claims 1-~~9~~6, wherein the transistors are double independent gate FET transistors which first and second independent gates are arranged laterally each one on one side of the channel region of the transistor.

~~11.~~8. The circuit according to any one of claims 1-~~9~~6 made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a base substrate by a buried insulating layer, wherein the first gate of each transistor is a front tri-gate surrounding all three sides of the channel of the transistor and the second control gate of each transistor is a back control gate formed in the base substrate below the channel of the transistor and separated from said channel by the buried insulating layer.

~~12.~~9. A system comprising at least one circuit according to any one of the preceding claims and a control circuit designed to modify the ~~inputs~~ signals provided to said at least one circuit so that the logic function provided by said at least one circuit can be changed in between the logic INV, NOR and NAND functions.

~~13.~~10. A wordline driver circuit comprising at least one pair of circuits according to ~~claims 3-4~~ claim 1 laid out in parallel, each circuit of the pair being intended to receive an input signal from a row address decoder and

providing at the output a signal intended to be used as a local wordline for a plurality of memory cells laid out as a row.

~~14.~~11. A memory incorporating a wordline driver circuit according to claim ~~13~~10.

~~15.~~12. A method for controlling a driver circuit according to claim ~~13~~10, wherein:

- in the active mode, the signal for biasing the second gates of the first circuit of a pair of circuits is complementary of the signal for biasing the second gates of the second circuit of the pair of circuits;
- in the inactive mode, the first terminal for application of a power supply potential and the signals for biasing the second gates of each of the circuits of the pair are in the OFF state.