What is claimed is:

1. A storage device comprising:

an external terminal serving dual purpose of an input terminal and a test terminal;

a control chip having a first control circuit and a first transfer switch electrically coupled to the first control circuit;

a first memory chip stacked on the control chip, and having a second control circuit and a second transfer switch electrically coupled to the second control circuit; and

a second memory chip stacked on the first memory chip, and having a third control circuit and a third transfer switch electrically coupled to the third control circuit,

wherein the control chip further has an input buffer whose input node is electrically coupled to the external terminal and whose output node is electrically coupled to the first control circuit, the second control circuit, and the third control circuit, and

the first memory chip further has a first connection switch whose one end is electrically coupled to the external terminal and whose another end is electrically coupled at least to the second transfer switch and the third transfer switch,

the storage device constitutes a first transmission path and a second transmission path, the first transmission path including a path from the external terminal to the first control circuit, the second control circuit, and the third control circuit with going through the input buffer, the second transmission path including a path from the external terminal to the second control circuit and the third control circuit with going through the first

connection switch, and

in a first mode, the control chip activates the first transmission path so as to make the external terminal function as the input terminal and, in a second mode, the control chip activates the second transmission path so as to make the external terminal function as the test terminal.

2. The storage device according to claim 1, wherein

the first mode includes an operation mode in which the control chip enables the input buffer and turns off the first connection switch such that a control signal is input from the external terminal via the input buffer to the first control circuit, the second control circuit and the third control circuit, and

the second mode includes a test mode in which the control chip disables the input buffer and turns on the first connection switch such that a test signal is input from the external terminal via the first connection switch to the second control circuit and the third control circuit or such that a monitor signal is output from the second control circuit or the third control circuit via the first connection switch to the external terminal.

3. The storage device according to claim 1, wherein

the second memory chip further has a second connection switch whose one end is at floating state and whose another end is electrically coupled at least to the second transfer switch and the third transfer switch.

4. The storage device according to claim 3, wherein

one end of the first transfer switch is electrically coupled to the external terminal,

another end of the first transfer switch is electrically coupled to the first control circuit, and

another end of the first connection switch is not electrically coupled to the first transfer switch and is electrically coupled to the second transfer switch and the third transfer switch.

5. The storage device according to claim 3, wherein

one end of the first transfer switch is electrically coupled to the first connection switch,

another end of the first transfer switch is electrically coupled to the first control circuit, and

another end of the first connection switch is electrically coupled to the first transfer switch, the second transfer switch and the third transfer switch.

6. The storage device according to claim 3, wherein

the first memory chip further has a fourth transfer switch whose one end is electrically coupled to the first connection switch and whose another end is electrically coupled to the first switch,

one end of the first transfer switch is electrically coupled to the fourth transfer switch, and

another end of the first transfer switch is electrically coupled to the first control circuit, and

another end of the first connection switch is electrically coupled to the second transfer switch and the third transfer switch and is electrically coupled via the fourth transfer switch to the first transfer switch.

7. The storage device according to claim 3, wherein

the second memory chip further has a fifth transfer

switch whose one end is electrically coupled to the second connection switch and whose another end is at floating state.

8. The storage device according to claim 1, further comprising an output terminal, and wherein

the control chip further has an output driver that outputs signals of the first memory chip or the second memory chip to the output terminal.

9. The storage device according to claim 8, wherein

the control chip further has a drive circuit that transfers signals transferred from the first memory chip or the second memory chip to the output driver.

10. The storage device according to claim 8, further comprising a third memory chip stacked on the second memory chip, wherein

the second memory chip puts together a signal of the second memory chip and a signal transferred from the third memory chip to transfer to the first memory chip, and

the output driver outputs a signal according to a signal transferred from the first memory chip to the output terminal.

11. The storage device according to claim 8, wherein

a signal line is connected, as a common signal line, to the first memory chip and the second memory chip, and a signal of each of the first memory chip and the second memory chip is output onto the common signal line via a second driver,

the control chip further has a drive circuit that includes a first current source electrically connected

between a power supply potential and the common signal line, and

the output driver is electrically connected between the common signal line and the output terminal.

12. The storage device according to claim 8, wherein

a signal line is connected, as a common signal line, to the first memory chip and the second memory chip, and a signal of each of the first memory chip and the second memory chip is output onto the common signal line via a third driver,

the control chip further has a drive circuit that includes a second current source electrically connected between a reference potential and the common signal line, and

the output driver is electrically connected between the common signal line and the output terminal.