

**SEMICONDUCTOR-METAL-ON-INSULATOR STRUCTURES, METHODS OF
FORMING SUCH STRUCTURES, AND SEMICONDUCTOR DEVICES
INCLUDING SUCH STRUCTURES**

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is related to co-pending U.S. Patent Serial No. Application 12/XXX,XXX filed on even date herewith and titled "FLOATING BODY CELL STRUCTURES, DEVICES INCLUDING SAME, AND METHODS FOR FORMING SAME" (attorney docket number 2269-9743US); co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "SEMICONDUCTOR DEVICES INCLUDING A DIODE STRUCTURE OVER A CONDUCTIVE STRAP AND METHODS OF FORMING SUCH SEMICONDUCTOR DEVICES" (attorney docket number 2269-9803US); co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "THYRISTOR-BASED MEMORY CELLS, DEVICES AND SYSTEMS INCLUDING THE SAME AND METHODS FOR FORMING THE SAME" (attorney docket number 2269-9804US); and co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "SEMICONDUCTOR CELLS, ARRAYS, DEVICES AND SYSTEMS HAVING A BURIED CONDUCTIVE LINE AND METHODS FOR FORMING THE SAME" (attorney docket number 2269-9819US), the disclosure of each of which is incorporated herein in its entirety by reference.

TECHNICAL FIELD

The present invention, in various embodiments, relates generally to semiconductor structures including a buried conductive material, and methods of forming such semiconductor structures. More specifically, embodiments of the present invention relate to a semiconductor-metal-on-insulator (SMOI) structure having a buried conductive material and methods of forming such structure. Additionally, the present invention relates to semiconductor devices including such SMOI structures and methods of forming such semiconductor devices.

BACKGROUND

One of the common trends in the electronics industry is the miniaturization of electronic devices. This is especially true for electronic devices operated through the use of semiconductor microchips. Microchips are commonly viewed as the brains of most electronic devices. In general, a microchip comprises a small silicon wafer upon which can be built millions or billions of nanoscopic electronic devices that are integrally configured to form electronic circuits. The circuits are interconnected in a unique way to perform a desired function.

With the desire to make high density microchips, it is necessary to decrease the size of the individual electronic devices and interconnects thereon. This movement also known as the so called "scale down" movement has increased the number and complexity of circuits on a single microchip.

Conventionally, electronic devices are formed side-by-side in a single plane on a common substrate, such as a silicon wafer. This side-by-side positioning, however, uses a relatively large amount of surface area, or "real estate," on the substrate. As a result, devices may be formed vertically in an effort to utilize less substrate area. In order to be competitive, such vertical devices are formed with high aspect ratios (i.e., the ratio of height to widths). However, as the aspect ratio of a device increases, it becomes increasingly difficult to satisfy both territory and electronic requirements of the corresponding interconnects. For this reason, simpler planar device scale downs dominate the industry in real practice to date.

A recent trend is to vertically stack semiconductor devices on a substrate. However, the stacking of semiconductor devices adds an additional complexity to connecting the components of the semiconductor device as well as providing efficient interconnects between the stacks.

Accordingly, there is a need for a method of forming a vertical semiconductor device which provides for competitive accessibility of interconnects to an electronic device in a stacked semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1-6 are cross-sectional views of an SMOI structure during various processing acts in accordance with one embodiment of the disclosure;

FIGs. 7-10 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 11-14 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 15-18 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 19-21 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 22-28 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 29-31 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 32-34 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIGs. 35-38 are cross-sectional views of an SMOI structure during various processing acts in accordance with another embodiment of the disclosure;

FIG. 39 is a perspective view of one embodiment of a semiconductor device including an SMOI structure of the disclosure;

FIG. 40 is a perspective view of another embodiment of a semiconductor device including an SMOI structure of the disclosure;

FIG. 41 is a cross-sectional view of another embodiment of a semiconductor device including an SMOI structure of the disclosure;

FIG. 42 is a perspective view of another embodiment of a semiconductor device including an SMOI structure of the disclosure; and

FIG. 43 is a perspective view of another embodiment of a semiconductor device including an SMOI structure of the disclosure.

FIG. 44 is a schematic block diagram illustrating one embodiment of an electronic system that includes a semiconductor device including an SMOI structure of the disclosure.

DETAILED DESCRIPTION

A semiconductor-metal-on-insulator (SMOI) structure and methods of forming such an SMOI structure. Such structures include, in one embodiment, an insulator material on a first semiconductor substrate, an amorphous silicon material bonded to the insulator material, a conductive material over the amorphous silicon material, and a second semiconductor substrate over the conductive material. Methods of forming such structures include, in one embodiment, forming an acceptor wafer including an insulator material formed over a first semiconductor substrate, forming a donor wafer including forming a conductive material over a precursor semiconductor substrate, forming an amorphous silicon material over the conductive material, and implanting ions into the precursor semiconductor substrate at a depth to form an implanted zone. The amorphous silicon material of the donor wafer may be bonded to the insulator material of the acceptor wafer. A portion of the precursor semiconductor substrate above the implanted zone may then be removed.

The SMOI structures formed in accordance with the various embodiments of the disclosure include an amorphous silicon material bonded to an insulator material, a conductive material, or an additional amorphous silicon material. The amorphous silicon material exothermically crystallizes or reacts with the insulator material, the conductive material, or the additional amorphous silicon material, which allows for silicon atom rearrangement, which can improve the bond strength at the interface between the amorphous silicon material and the insulator material, the conductive material, or the additional silicon material. As such, the bond created between the amorphous silicon material and the at least one of the insulator material, the conductive material, and the additional amorphous silicon material may be substantially stronger than a bond created between two insulator materials, such as two oxide materials. Additionally, the bonding of the amorphous silicon material to the insulator material may occur at a relatively low temperature, such as at room temperature (from approximately 20°C to approximately 25°C), and, thus, reduces the risk of damage to any underlying devices formed on the first semiconductor substrate. Bonding of the amorphous silicon material to the at least one of the insulator material, the conductive material, and the additional amorphous silicon material is described in greater detail below. The SMOI structures formed in accordance with the various embodiments of the disclosure

may also include a conductive material disposed between the insulator material and the second semiconductor substrate. The conductive material is buried beneath the second semiconductor substrate. The conductive material may be used, in some embodiments, to form an interconnect, such as a word line or a bit line, or to form a metal strap. Such an interconnect may be used to facilitate access to a semiconductor device formed in the second semiconductor substrate.

The SMOI structures formed in accordance with various embodiments of the disclosure may be used to fabricate a variety of semiconductor devices, such as an integrated circuit including a logic device formed in/on the first semiconductor substrate and a memory device formed in/on the second semiconductor substrate. Since the conductive material is buried beneath the second semiconductor substrate, devices formed on the second semiconductor substrate may be formed in relatively few process acts, as described in greater detail below. Additionally, the devices formed on/in the second semiconductor substrate may be self-aligned with the underlying interconnect and/or source and drain contacts, thus eliminating the need for a separate electrical contact. Furthermore, since a logic device may be formed on the first semiconductor substrate before the SMOI structure and the memory device are formed, the memory device is not exposed to the processing conditions used for the formation of the logic device. By forming such vertical, self-aligned, stacked integrated circuits, the cell size may be reduced, which provides for increased cache memory density.

The following description provides specific details, such as material types and processing conditions, in order to provide a thorough description of embodiments of the disclosure. However, a person of ordinary skill in the art will understand that embodiments of the present invention may be practiced without employing these specific details and in conjunction with conventional fabrication techniques. In addition, the description provided herein does not form a complete process flow for manufacturing a semiconductor device including the SMOI structure. Only those process acts and structures necessary to understand the embodiments of the disclosure are described in detail below. Additional acts to form a complete semiconductor device including the SMOI structure according to an embodiment of the invention may be performed by conventional techniques. In addition, it is understood that the methods described herein may be repeated as many times as desired to form multiple, stacked SMOI structures.

The materials described herein may be formed by any suitable technique including, but not limited to, spin coating, blanket coating, chemical vapor deposition ("CVD"), plasma enhanced chemical vapor deposition ("PECVD"), atomic layer deposition ("ALD"), plasma enhanced ALD, or physical vapor deposition ("PVD"). Alternatively, materials may be grown *in situ*. A technique suitable for depositing or growing a particular material may be selected by a person of ordinary skill in the art. While the materials described and illustrated herein may be formed as layers, the materials are not limited thereto and may be formed in other three-dimensional configurations.

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the invention. However, other embodiments may be utilized, and structural, logical, and electrical changes may be made without departing from the scope of the invention. The illustrations presented herein are not meant to be actual views of any particular system, logic device, memory cell, or semiconductor device, but are merely idealized representations which are employed to describe embodiments of the disclosure. The drawings presented herein are not necessarily drawn to scale. Additionally, elements common between drawings may retain the same numerical designation.

Referring now to the drawings, where like elements are designated by like reference numerals, FIGs. 1 through 6 are partial cross-sectional views of a method of forming an embodiment of an SMOI structure 30 (FIG. 6) including a conductive material 204, which is buried. The SMOI structure 30 is formed by bonding an acceptor wafer 10 (FIG. 1) and a donor wafer 20 (FIG. 2). FIG. 1 depicts the acceptor wafer 10. The acceptor wafer 10 may include a first semiconductor substrate 102 having an insulator material 104 formed thereon. The first semiconductor substrate 102 may include a fabrication substrate, such as a full or partial wafer of semiconductor material (*e.g.*, silicon, gallium arsenide, indium phosphide, etc.), a full or partial silicon-metal-on-insulator (SMOI) type substrate, such as a silicon-on-glass (SOG), silicon-on-ceramic (SOC), or silicon-on-sapphire (SOS) substrate, or any other known, suitable fabrication substrate. As used herein, the term "wafer" includes conventional wafers as well as other bulk semiconductor substrates. The first semiconductor

substrate 102 may be doped or undoped. An at least partially fabricated logic device (not shown), such as a CMOS device, may optionally be present on the first semiconductor substrate 102 and may be formed by conventional techniques. In one embodiment, the first semiconductor substrate 102 is bulk crystalline silicon.

5 The insulator material 104 may be a dielectric material including, by way of non-limiting example, silicon dioxide, borophosphosilicate glass (BPSG), borosilicate glass (BSG), phosphosilicate glass (PSG) or the like. In one embodiment, the insulator material 104 is a buried oxide. The insulator material 104 may be from about 500 Å to about 2 μm thick, such as from about 1000 Å to about 2000 Å. Techniques for deposition and *in situ*
10 growth of such dielectric materials are known in the art and may include, for example, chemical vapor deposition (CVD), such as low pressure CVD or plasma enhanced CVD, atomic layer deposition (ALD), spin-on deposition, thermal decomposition, or thermal growth. The insulator material 104 includes an upper surface 106.

FIG. 2 is a partial cross-sectional view of one embodiment of the donor wafer 20 used
15 to form the SMOI structure 30 (FIG. 6). The donor wafer 20 may include a precursor semiconductor substrate 202 having a conductive material 204 and an amorphous silicon material 206 formed thereon. In some embodiments, a polysilicon material or another amorphous material, such as amorphous germanium, may be substituted for the amorphous silicon material 206. The precursor semiconductor substrate 202 may be, for example, one
20 of the fabrication substrates mentioned above for use as first semiconductor substrate 102. In one embodiment, the precursor semiconductor substrate 202 is a silicon substrate, such as a crystalline silicon substrate. The precursor semiconductor substrate 202 may be doped or undoped. The conductive material 204 may be a low resistivity material including, but not limited to, a phase change material, titanium, titanium silicide, titanium oxide, titanium
25 nitride, tantalum, tantalum silicide, tantalum oxide, tantalum nitride, tungsten, tungsten silicide, tungsten oxide, tungsten nitride, other metal, metal silicide, metal oxide, or metal nitride materials, or combinations thereof, including multiple, different conductive materials. In one embodiment, the conductive material 204 may be formed from titanium nitride because titanium nitride has good adherence or adhesion to many materials, such as the
30 material used as the precursor semiconductor substrate 202. Titanium nitride also has a high melting point (about 3000°C), which makes it unaffected by high processing temperatures.

Titanium nitride also makes excellent ohmic contact with other conductive materials.

Titanium nitride is also commonly used in semiconductor fabrication and, therefore, may easily be incorporated into conventional fabrication processes. In one embodiment, the conductive material 204 is a titanium-rich titanium nitride, such as metal mode titanium

5 nitride (MMTiN). The conductive material 204 may also be formed from multiple conductive materials. In one embodiment, the conductive material 204 is a MMTiN material over the precursor semiconductor substrate 202 and a tungsten silicide material over the MMTiN material. In another embodiment, the conductive material 204 may be formed from a metal, such as titanium, tungsten or aluminum, with a layer of titanium material formed
10 thereon. The thickness of the conductive material 204 may be optimized, depending on the material, to provide a low ohmic contact between the conductive material 204 and the precursor semiconductor substrate 202. For example, if the conductive material 204 is titanium nitride, such as MMTiN, the conductive material 204 may have a thickness of from about 10 nm to about 50 nm. The conductive material 204 may be formed by a deposition
15 technique known in the art, such as, for example, atomic layer deposition (ALD), chemical vapor deposition (CVD), or plasma vapor deposition (PVD).

The amorphous silicon material 206 may be formed over the conductive material 204 by a deposition technique known in the art, such as, for example, ALD, CVD, or PVD. In one embodiment, the amorphous silicon material 206 may be formed on the conductive
20 material 204 by PVD, followed by chemical mechanical planarization (CMP). The amorphous silicon material 206 may be of sufficient thickness to adhere to the insulator material 104 of the acceptor wafer 10 as described in greater detail below. For example, the thickness of the amorphous silicon material 206 may be from about 10 nm to about 50 nm. The amorphous silicon material 206 includes a surface 212.

25 As depicted in FIG. 2, the donor wafer 20 may also include a cleave portion 208 formed by implanting an atomic species into the precursor semiconductor substrate 202. The atomic species may be hydrogen ions, ions of rare gases, also termed inert or noble gases, or ions of fluorine. The atomic species may be implanted into the precursor semiconductor substrate 202 of the donor wafer 20 to form an implanted zone 210. The atomic species may
30 be implanted into the precursor semiconductor substrate 202 prior to formation of the conductive material 204 thereon, after formation of the conductive material 204 thereon, or

after formation of the amorphous silicon material 206 thereon. The implanted zone 210 may be formed at a desired depth in the precursor semiconductor substrate 202, which is dependent on parameters, such as implant dose and energy of the atomic species, as known in the art. The depth of the implanted zone 210 may correspond to the thickness of a second semiconductor substrate 202' of the SMOI structure 30 (FIG. 6). The implanted zone 210 may include microbubbles or microcavities including the implanted atomic species, which provide a weakened region within the precursor semiconductor substrate 202. The donor wafer 20 may be thermally treated at a temperature above that at which implantation is effected, but below the melting temperature of the conductive material 204, to effect crystalline rearrangement in the donor wafer 20 and coalescence of the microbubbles or microcavities. As described below, the donor wafer 20 may be cleaved at the implanted zone 210, forming the second semiconductor substrate 202' on the SMOI structure 30 (FIG. 6) and cleave portion 208. For clarity, the term "second semiconductor substrate" is used herein to refer to the semiconductor structure after removal of the cleave portion 208, while the term "precursor semiconductor substrate" is used herein to refer to the semiconductor structure before removal of the cleave portion 208.

As shown in FIG. 3, the donor wafer 20 may be superposed onto the acceptor wafer 10 such that the amorphous silicon material 206 of the donor wafer 20 is in contact with the insulator material 104 of the acceptor wafer 10. The amorphous silicon material 206 of the donor wafer 20 may then be bonded to the insulator material 104 of the acceptor wafer 10 by exposure to heat. Prior to bonding the donor wafer 20 to the acceptor wafer 10, at least one of the surface 212 of the amorphous silicon material 206 and the upper surface 106 of the insulator material 104 may, optionally, be treated to improve the bond strength between the amorphous silicon material 206 and the insulator material 104. Such treatment techniques are known in the art and may include chemical, plasma, or implant activations. For example, the upper surface 106 of the insulator material 104 may be treated with a dilute ammonia hydroxide or hydrogen fluoride solution. The surface 212 of the amorphous silicon material 206 may also be exposed to a plasma of, for example, argon, to form a plasma-activated surface. Activating at least one of the surface 212 of the amorphous silicon material 206 and the upper surface 106 of the insulator material 104 may increase the kinetics of the subsequent bonding therebetween due to an increased mobility of ionic species (for example,

hydrogen) created on the surface 212 of the amorphous silicon material 205 and the upper surface 106 of the insulator material 104.

As shown in FIG. 4, the amorphous silicon material 206 of the donor wafer 20 may be contacted and bonded with the insulator material 104 of the acceptor wafer 10 to form a precursor of the SMOI structure 30. The amorphous silicon material 206 may be bonded to the insulator material 104 by, for example, heating the SMOI structure 30 to a temperature of less than about 600°C, such as from about 300°C to about 400°C. If the insulator material 104 is formed from silicon dioxide, silicon-oxide bonds may form between the amorphous silicon material 206 and the insulator material 104. Because the conductive material 204 may be formed of a metal or other heat sensitive material, the temperature to which the SMOI structure 30 is exposed may be less than the melting point of the conductive material 204. The amorphous silicon material 206 and the insulator material 104 may also be bonded without heat, such as at ambient temperature (from about 20°C to about 25°C). Pressure may also be applied to the donor wafer 20 and the acceptor wafer 10 to bond the amorphous silicon material 206 to the insulator material 104. Once the donor wafer 20 is bonded to the acceptor wafer 10, the conductive material 204 from the donor wafer 20 may form a buried conductive material, which is disposed between the insulator material 104 and the precursor semiconductor substrate 202.

To form the SMOI structure 30 (FIG. 6), the cleave portion 208 may be removed from the precursor semiconductor substrate 202, as shown in FIG. 5. The cleave portion 208 may be removed by techniques known in the art, such as by applying a shear force to the implanted zone 210 or by applying heat or a jet gas stream at the implanted zone 210. The hydrogen or other ions implanted in the implanted zone 210 produce a weakened region in the precursor semiconductor substrate 202, which is susceptible to cleavage. The remaining portion of the second semiconductor substrate 202' may have a thickness, for example, of from about 50 nm to about 500 nm (from about 500 Å to about 5000 Å). A surface 302 of the SMOI structure 30, exposed after removing the cleave portion 208, may be rough and jagged. The exposed surface 302 of the SMOI structure 30 may be smoothed to a desired degree in order to facilitate further processing of the SMOI structure 30, as described below. The exposed surface 302 of the SMOI structure may be smoothed according to conventional

techniques such as, for example, one or more of grinding, wet etching, chemical-mechanical polishing (CMP), and planar reactive ion etching (RIE).

The SMOI structure 30 and the other structures described below may be formed by modification of SMART-CUT[®] layer transfer technology. The SMART-CUT[®] layer transfer technology is described in detail in, for example, U.S. Patent No. RE 39,484 to Bruel, U.S. Patent No. 6,303,468 to Aspar et al., U.S. Patent No. 6,335,258 to Aspar et al., U.S. Patent No. 6,756,286 to Moriceau et al., U.S. Patent No. 6,809,044 to Aspar et al., U.S. Patent No. 6,946,365 to Aspar et al., and U.S. Patent Application Publication No. 2006/0099776 to Dupont. However, other processes suitable for manufacturing an SMOI substrate may also be used, if sufficiently low process temperatures are maintained. In conventional implementation of the SMART-CUT[®] layer transfer technology, donor wafers and acceptor wafers are bonded together using a high temperature anneal. The temperature used to bond the donor and acceptor wafers is from about 1000°C to about 1300°C. However, due to the presence of the conductive material 204 in the SMOI structures described herein, the SMOI structures of the disclosure may, in some circumstances, be unable to withstand exposure to such temperatures without thermal damage. Accordingly, as described above, lower temperatures may be used to bond and acceptor wafer 10 and donor wafer 20.

FIG. 6 is an illustration of the SMOI structure 30 after the exposed surface 302 has been smoothed. Once the donor wafer 20 is bonded to the acceptor wafer 10 and the exposed surface 302 smoothed, then a semiconductor device, such as a memory cell, may be formed on and/or within the second semiconductor substrate 202' of the SMOI structure 30. As described below, the conductive material 204 of the SMOI structure 30 may function as, for example, an interconnect, such as a bit line or word line, as a gate, or as a metal strap.

FIGs. 7 through 10 are partial cross-sectional views of a method of forming an embodiment of an SMOI structure 50 (FIG. 10) including a conductive silicide material 410, which is buried. FIG. 7 illustrates an acceptor wafer 11 used to form the SMOI structure 50 (FIG. 10). The acceptor wafer 11 may be substantially similar to the acceptor wafer 10 described above and may be formed as described above regarding FIG. 1, with the exception that the amorphous silicon material 206 may be formed over the insulator material on the acceptor wafer 10. As shown in FIG. 7, the acceptor wafer 10 may include the amorphous

silicon material 206 formed over the insulator material 104 and the insulator material 104 formed over the first semiconductor substrate 102.

FIG. 8 is a partial cross-sectional view of one embodiment of a donor wafer 40 used to form the SMOI structure 50 (FIG. 10). The donor wafer 40 may be substantially similar to the donor wafer 20 described above and may be formed as described above regarding FIG. 2, with the exception that the donor wafer 40 may include an optional non-reactive conductive material 402 and a reactive conductive material 404 instead of conductive material 204 (FIG. 2), and the amorphous silicon material 206 (FIG. 2) is not formed on the donor wafer 40.

The non-reactive conductive material 402 may be formed of, for example, a metal nitride, such as titanium nitride. However, any conductive material that will not chemically react with the reactive conductive material 404 or a reaction product thereof may be used. The thickness of the non-reactive conductive material 402 may be relatively thin compared to the thickness of the reactive conductive material 404. For example, the non-reactive conductive material 402 may have a thickness of from about 20 Å to about 200 Å. The reactive conductive material 404 may be formed of a metal capable of reacting with the amorphous silicon material 206 or acts as a catalyst for crystallizing the amorphous silicon material 206. In one embodiment, the reactive conductive material 404 is titanium. The reactive conductive material 404 may have a thickness of from about 200 Å to about 500 Å. The non-reactive conductive material 402 and the reactive conductive material 404 may be formed by a deposition technique known in the art, such as, for example, ALD, CVD, or PVD.

As shown in FIG. 9, the donor wafer 40 may be superposed onto the acceptor wafer 10 and bonded thereto and the cleave portion 208 (FIG. 8) removed, as previously described regarding FIGs. 3-6. The resulting SMOI structure 50 may include the first semiconductor substrate 102, the insulator material 104, the amorphous silicon material 206, the reactive conductive material 404, the non-reactive conductive material 402, and the second semiconductor substrate 202'.

As shown in FIG. 10, the SMOI structure 50 may be annealed so that the reactive conductive material 404 chemically reacts with the amorphous silicon material 206, forming the conductive silicide material 410, which is buried beneath the non-reactive conductive material 402. The reactive conductive material 404 may be formed from titanium, which

reacts with the amorphous silicon material 206 to form titanium silicide as the conductive silicide material 410. The reactive conductive material 404 and the non-reactive conductive material 402 may also be a single material, such as titanium-rich titanium nitride (MMTi). Excess titanium in the titanium-rich titanium nitride may react with the amorphous silicon material 206, forming the conductive silicide material 410. Annealing the SMOI structure 50 to form the conductive silicide material 410 may occur at a temperature of, for example, from about 600°C to about 800°C. The bond strength between the conductive silicide material 410 and the insulator material 104 may be greater than that between the amorphous silicon material 206 and the insulator material 104. The conductive silicide material 410 may provide a lower resistance to the SMOI structure 50 than the reactive conductive material 404.

FIGs. 11 through 14 are partial cross-sectional views of a method of forming an embodiment of an SMOI structure 70 (FIG. 14) including a conductive material, which is buried beneath a doped semiconductor substrate. FIG. 11 illustrates an acceptor wafer 10, which is a substantial duplication of FIG. 1 and may be formed as described above regarding FIG. 1. As shown in FIG. 11, the acceptor wafer may include the insulator material 104 formed over the first semiconductor substrate 102.

FIG. 12 is a partial cross-sectional view of one embodiment of a donor wafer 60 used to form the SMOI structure 70 (FIG. 14). The donor wafer 60 may include a precursor semiconductive substrate 202 similar to the donor wafer 20 described above and may be formed as described above regarding FIG. 2. The precursor semiconductive substrate 202 may be doped and activated, as known in the art, to form a P+ doped region 602, an N- doped region 604, and an N+ doped region 606. In one embodiment, the precursor semiconductive substrate 202 may be doped using a high temperature process since the precursor semiconductive substrate does not yet include a MMTiN material 610 (FIG. 13) which may be damaged by such high temperature processes. In another embodiment, the P+ doped region 602 may be formed after the SMOI device 70 (FIG. 14) has been formed using a low temperature process for better dopant profile control. While FIG. 12 is depicted as including a particular order of the P+ doped region 602, the N- doped region 604, and the N+ doped region 606, it is understood that one of ordinary skill in the art may choose any combination of doped regions to achieve desired functions for the SMOI structure 70 (FIG. 14). Because

the donor wafer 60 has two exposed surfaces from which the desired dopant may be implanted, the depth and concentration (i.e. highly doped or lightly doped) of the doped regions 602, 604, 606 may be more easily and accurately controlled than if the doped regions were formed after the donor wafer 60 is bonded to the acceptor wafer 10. As shown in FIG.

5 12, a silicide material 608 may be formed over the precursor semiconductor substrate 202, such as over the N⁺ doped region 606. The silicide material 608 may be formed by forming reactive conductive material over the precursor semiconductor substrate 202 so that the reactive conductive material reacts with the precursor semiconductor substrate 202 to form the silicide material 608. The silicide material 608 may have a low ohmic contact with the precursor semiconductor substrate 202. A metal mode titanium nitride (MMTiN) material 10 may be formed over the silicide material 608. MMTiN material 610 and tungsten silicide material 612 may be formed by a deposition technique known in the art, such as, for example, ALD, CVD, or PVD. The thickness of the silicide material 608 may be relatively thin compared to the thickness of the MMTiN material 610. For example, the silicide material 15 608 may have a thickness of from about 50 Å to about 500 Å. The MMTiN material 610 may have a thickness of from about 500 Å to about 1000 Å. Also, as depicted in FIG. 12, the cleave portion 208 may be formed by implanting an atomic species into the precursor semiconductor substrate 202, forming the implanted zone 210 as previously described regarding FIG. 2. As shown in FIG. 12, the implanted zone 210 may be formed within the 20 P⁺ doped region 602 of the precursor semiconductor substrate 202. The silicide material 608 and the MMTiN material 610 may have a substantially minimal impact on the implanting of the atomic species when forming the implanted zone 210.

As shown in FIG. 13, a tungsten silicide material 612 and an amorphous silicon material 206 may be formed over the silicide material 608. The tungsten silicide material 612 25 may be formed by a deposition technique known in the art, such as, for example, ALD, CVD, or PVD. The tungsten silicide material 612 may be a better conductor than the MMTiN nitride material 610. In some embodiments, the tungsten silicide material 612 may be formed over the titanium silicide material 612 and MMTiN material 610 after the implanted zone 210 is formed.

30 As shown in FIG. 14, the donor wafer 60 may be superposed onto the acceptor wafer 10 and bonded thereto and the cleave portion 208 (FIG. 13) removed, as previously described

regarding FIGs. 3-6. The resulting SMOI structure 70 may include the first semiconductor substrate 102, the insulator material 104, the amorphous silicon material 206, the tungsten silicide material 612, the MMTiN material 610, the silicide material 608, and the second semiconductor substrate 202' including the N+ doped region 606, the N- doped region 604, and the P+ doped region 602. In some embodiments, a second conductive material (not shown) may be formed over the P+ doped region 602 to form a top electrode which may be used to form a semiconductor device as described in greater detail below.

FIGs. 15 through 18 are partial cross-sectional views of another method of forming an embodiment of an SMOI structure 90 (FIG. 18) including a doped semiconductor material.

FIG. 15 is a substantial duplication of FIG. 1 and may be formed as described above regarding FIG. 1. As shown in FIG. 15, the acceptor wafer 10 includes the insulator material 104 formed over the first semiconductor substrate 102.

FIG. 16 is a partial cross-sectional view of one embodiment of a donor wafer 80 used to form the SMOI structure 90 (FIG. 18). The donor wafer 80 may be substantially similar to the donor wafer 20 described regarding FIG. 2 above and may be formed as described above regarding FIG. 2, with the exception that the donor wafer 80 may include a doped semiconductive material 802 disposed between the precursor semiconductor substrate 202 and the conductive material 204. The doped semiconductive material 802 may be formed of, for example, at least one of germanium (Ge), silicon carbide (SiC) and gallium nitride (GaN).

The precursor semiconductor substrate 202 may be doped to form at least one P+ or N+ doped region 804. The doped semiconductive material 802 may also be doped to form a P doped region 806 and an N doped region 808. In one example, the P doped region 806 may include a P doped silicon carbide material adjacent the P+ or N+ doped region 804 of the precursor semiconductor substrate 202 and the N-doped region 808 may include an N doped silicon carbide material adjacent the P doped region 806. The doped semiconductive material 802 may be formed on the precursor semiconductor substrate 202 using conventional deposition or *in situ* growth techniques and may include, for example, chemical vapor deposition (CVD), such as low pressure CVD or plasma enhanced CVD, atomic layer deposition (ALD), spin-on deposition, thermal decomposition, or thermal growth. The conductive material 204 and the amorphous silicon material 206 may be deposited over the doped semiconductive material 802, and the precursor semiconductor substrate 202 may be

implanted with an atomic species to form the implanted zone 210 and the cleave portion 208 as described above regarding FIG. 2.

As shown in FIG. 17, the donor wafer 80 may be superposed onto the acceptor wafer 10 and bonded thereto and the cleave portion 208 removed as previously described regarding FIGS. 3-6. The resulting SMOI structure 90 includes the first semiconductor substrate 102, the insulator material 104, the amorphous silicon material 206, the conductive material 204, the doped semiconductive material 802 including the N doped region 808 and the P doped region 806, and the second semiconductor substrate 202' including the P+ or N+ doped region 804. As shown in FIG. 18, the second semiconductor substrate 202' may be polished using techniques known in the art, such as CMP.

FIGS. 19 through 21 are partial cross-sectional views of another method of forming an embodiment of an SMOI structure 120 (FIG. 21) including the insulator material 104 and a high-k dielectric material 112. FIG. 19 is a substantial duplication of FIG. 1 and may be formed as described above regarding FIG. 1. As shown in FIG. 19, the acceptor wafer 10 includes the insulator material 104 formed over the first semiconductor substrate 102.

FIG. 20 is a partial cross-sectional view of one embodiment of a donor wafer 110 used to form the SMOI structure 120 (FIG. 21). The donor wafer 110 may be substantially similar to the donor wafer 20 described regarding FIG. 2 above and may be formed as described above regarding FIG. 2, with the exception that the donor wafer 110 includes a high-k dielectric material 112 disposed between the precursor semiconductor substrate 202 and the conductive material 204. The high-k dielectric material 112 may be formed of, for example, silicon dioxide, hafnium oxide, and other oxides, silicates, or aluminates of zirconium, aluminum, lanthanum, strontium, titanium, or combinations thereof including but not limited to Ta_2O_5 , ZrO_2 , HfO_2 , TiO_2 , Al_2O_3 , Y_2O_3 , La_2O_3 , HfSiO_x , ZrSiO_x , LaSiO_x , YSiO_x , ScSiO_x , CeSiO_x , HfLaSiO_x , HfAlO_x , ZrAlO_x , and LaAlO_x . In addition, multi-metallic oxides may be used, as may hafnium oxynitride, iridium oxynitride and other high-k dielectric materials in either single or composite layers. The high-k dielectric material 112 may be formed on the precursor semiconductor substrate 202 using conventional deposition or *in situ* growth techniques and may include, for example, chemical vapor deposition (CVD), such as low pressure CVD or plasma enhanced CVD, atomic layer deposition (ALD), spin-on deposition, thermal decomposition, or thermal growth.

Optionally, the donor wafer 110 may also include a metal 113 and a doped region 115. The metal 113 may include, for example, a reactive conductor such as metal mode titanium (MMTi), titanium (Ti), tantalum (Ta), cobalt (Co), and nickel (Ni). The conductive material 204 and the amorphous silicon material 206 may be deposited over the high-k dielectric material 112 and the precursor semiconductor substrate 202 may be implanted with an atomic species to form the implanted zone 210 and the cleave portion 208 as described above regarding FIG. 2.

As shown in FIG. 21, the donor wafer 110 may be superposed onto the acceptor wafer 10 and bonded thereto and the cleave portion 208 (FIG. 20) removed as previously described regarding FIGs. 3-6. The resulting SMOI structure 120 includes the substrate 102, an insulator material 104, the amorphous silicon material 206, the conductive material 204, the high-k dielectric material 112 and the second semiconductor substrate 202'.

FIGs. 22 through 28 are cross-sectional views of a method of forming another embodiment of an SMOI structure 140 (FIG. 28) including a patterned conductive material 204'. FIG. 22 is a substantial duplication of FIG. 1 and may be formed as described above regarding FIG. 1. As shown in FIG. 22, the acceptor wafer 10 includes the insulator material 104 formed over the first semiconductor substrate 102.

FIG. 23 is a partial cross-sectional view of one embodiment of a donor wafer 130 used to form the SMOI structure 140 (FIG. 28). The donor wafer 130 includes the precursor semiconductor substrate 202 having the conductive material 204 and a cap material 132 formed thereon. The cap material 132 may be formed of a dielectric material, such as a nitride material or an oxide material. The cap material 132 may be formed by deposition techniques known in the art including, but not limited to, ALD, CVD, or PVD.

As shown in FIG. 24, the cap material 132 and the conductive material 204 may be patterned to form at least one structure 134 including the patterned cap material 132' and the patterned conductive material 204'. The cap material 132 and the conductive material 204 may be patterned using techniques known in the art, such as photoresist masking and anisotropic etching. Alternatively, in some embodiments, the patterned cap material 132' and the patterned conductive material 204' may be formed as the at least one structure 134 using a damascene flow process, which is known in the art and is, therefore, not described in detail herein. As shown in FIG. 25, an interlevel dielectric material 136 may be deposited over the

at least one structure 134 of the patterned cap material 132' and patterned conductive material 204'. The interlevel dielectric material 136 may be used to electrically isolate the at least one structure 134 from an adjacent structure 134. As shown in FIG. 26, the interlevel dielectric material 136 may be removed to expose an upper surface of the patterned cap material 132',
 5 such as by CMP, as known in the art. The patterned cap material 132' may act as a CMP stop.

As shown in FIG. 27, the amorphous silicon material 206 may be formed over the interlevel dielectric material 136 and the patterned cap material 132'. The donor wafer 130 may also be implanted with an atomic species forming the implanted zone 210 and the cleave
 10 portion 208 as previously described regarding FIG 2. As shown in FIG. 28, the donor wafer 130 may be superposed onto the acceptor wafer 10 and bonded thereto and the cleave portion 208 removed as previously described regarding FIGs. 3-6. The resulting SMOI structure 140 includes the first semiconductor substrate 102, the insulator material 104, the amorphous silicon material 206, at least one structure 134 of the patterned cap material 132' and the
 15 conductive material 204', the at least one structure 134 being electrically isolated by the interlevel dielectric material 136, and the second semiconductor substrate 202'. Because the pillars 134 including the conductive material 204' are patterned and separated by the interlevel dielectric material 136, the conductive material 204' may be used as an interconnect, such as a word line or a bit line without further processing, as described in
 20 greater detail below.

In additional embodiments, the conductive material 204 may be formed on an acceptor wafer rather than a donor wafer. For example, FIGs. 29-31 illustrate partial cross-sectional views of another method of forming an embodiment of an SMOI structure 170 (FIG. 31) including the conductive material 204. As shown in FIG. 29, an acceptor
 25 wafer 150 includes the first semiconductor substrate 102, the insulator material 104, and the conductive material 204. The acceptor wafer 150 may, optionally, include a bonding material 152. The bonding material 152 (if present) may be either an amorphous silicon material, as previously described, or the bonding material 152 may be an oxide material, such as silicon dioxide. In some embodiments, the conductive material 204 may be patterned and filled with
 30 an interlevel dielectric material (not shown) as described above regarding FIGs. 22-28.

FIG. 30 is a partial cross-sectional view of one embodiment of a donor wafer 160 used to form the SMOI structure 170 (FIG. 31). The donor wafer 160 may include the precursor semiconductor substrate 202 and the amorphous silicon material 206. The donor wafer 160 may be implanted with an atomic species forming the implanted zone 210 and the cleave portion 208 as previously described regarding FIG 2.

As shown in FIG. 31, the donor wafer 160 may be superposed onto the acceptor wafer 150 and bonded thereto, and the cleave portion 208 may be removed as previously described regarding FIGs. 3-6. The resulting SMOI structure 170 includes the first semiconductor substrate 102, the insulator material 104, the conductive material 204, the bonding material 152 (if present) bonded to the amorphous silicon material 206, and the second semiconductor substrate 202'.

In additional embodiments, multiple SMOI structures may be formed by creating multiple layers of silicon material on a donor wafer. For example, FIGs. 32-34 illustrate partial cross-sectional views of another method of forming an embodiment of an SMOI structure 200 (FIG. 32) including a conductive material 204. As shown in FIG. 32, an acceptor wafer 180 includes the first semiconductor substrate 102, the insulator material 104, and the conductive material 204.

FIG. 33 is a partial cross-sectional view of one embodiment of a donor wafer 190 used to form the SMOI structure 200 (FIG. 34). The donor wafer 190 may include the precursor semiconductor substrate 202, at least one portion of a silicon-germanium (SiGe) material 192, and at least one portion of an epitaxial (EPI) silicon material 194. The SiGe material 192 and EPI silicon material 194 may be formed by methods known in the art and at any desired thickness. Additionally, the SiGe material 192 and the EPI silicon material 194 may be doped or undoped. While FIG. 33 shows one portion of the SiGe material 192 and one portion of the EPI silicon material 194, multiple portions may be present by forming alternating portions of the SiGe material 192 and the EPI silicon material 194. In some embodiments, the amorphous silicon material 206, illustrated in dashed lines, may be optionally formed over the uppermost portion of the EPI silicon material 194 or the SiGe material 192. Alternatively, in some embodiments, the amorphous silicon material 206 may be omitted and the uppermost portion of the EPI silicon material 194 or the SiGe material 192 may be bonded to the acceptor wafer 180. The donor wafer 190 may also be implanted with

an atomic species, forming the implanted zone 210 and the cleave portion 208 as previously described regarding FIG 2.

As shown in FIG. 34, the donor wafer 190 may be superposed onto the acceptor wafer 180 and bonded thereto, and the cleave portion 208 may be removed as previously described regarding FIGs. 3-6. The resulting SMOI structure 200 includes the first semiconductor substrate 102, the insulator material 104, the conductive material 204, the amorphous silicon material 206 (if present), the at least one portion of the EPI silicon material 194, the at least one portion of the SiGe material 192, and the second semiconductor substrate 202'. While FIG. 23 is depicted as bonding the amorphous silicon material 206 to the conductive material 204, either of the EPI silicon material 194, the SiGe material 192, or the amorphous silicon material 206 (if present) may be used to bond the donor wafer 190 to the acceptor wafer 180. Once the SMOI structure 200 is formed, portions of the SiGe material 192 may be removed, such as, for example, utilizing a wet undercut etch. The portions of the SiGe material 192 that are removed may then be back filled with a dielectric material (not shown), such as an oxide material or the removed portions may be left unfilled, forming an air gap (not shown). Replacing portions of the SiGe material 192 with a dielectric material or an air gap may be used to form multiple SMOI structures on the substrate 102. In still further embodiments, the SMOI structure 200 may be formed without the conductive material 204, thus forming multiple SMOI structures on the substrate 102 without the conductive material 204.

In additional embodiments, the SMOI structure may be formed with a multi-portion buried dielectric material. For example, FIGs. 35-38 illustrate partial cross-sectional views of another method of forming an embodiment of an SMOI structure 250 (FIG. 38) including a multi-portion buried dielectric material 226. As shown in FIG. 35, an acceptor wafer 220 includes the first semiconductor substrate 102, the insulator material 104, at least one portion of an oxide material 222, and at least one portion of a nitride material 224. In some embodiments, the insulator material 104 may, optionally, be omitted. The oxide material 222 and the nitride material 224 may be formed in alternating portions. The oxide material 222 and the nitride material 224 may be formed by methods known in the art and at any desired thickness. While FIG. 35 is illustrated as including two portions of the oxide material 222 alternating with two portions of the nitride material 224, it is understood that any number of portions of oxide material 222 and nitride material 224 may be present.

FIG. 36 is a partial cross-sectional view of one embodiment of a donor wafer 230 used to form the SMOI structure 250 (FIG. 38). The donor wafer 230 may be substantially similar to the donor wafer 20 described above in FIG. 2 and may be formed as described above regarding FIG. 2. As shown in FIG. 36, the donor wafer 230 may include the precursor semiconductor substrate 202 and the amorphous silicon material 206. The donor wafer 230 may also be implanted with an atomic species forming the implanted zone 210 and the cleave portion 208.

As shown in FIG. 37, the donor wafer 230 may be superposed onto the acceptor wafer 220 and bonded thereto, and the cleave portion 208 may be removed as previously described regarding FIGs. 3-6. A resulting SMOI structure 240 includes the first semiconductor substrate 102, the insulator material 104, at least one portion of the oxide material 222, at least one portion of the nitride material 224, the amorphous silicon material 206, and the second semiconductor substrate 202'. While FIG. 37 is depicted as bonding the amorphous silicon material 206 to the at least one portion of the oxide material 222, any of the at least one portion of the nitride material 224, the at least one portion of the oxide material 222, or an additional amorphous silicon material (not shown) may be used to bond the donor wafer 230 to the acceptor wafer 220. Once the SMOI structure 240 is formed, portions of the nitride material 224 may be selectively removed, such as, for example, by a selective undercut utilizing a wet etch. The portions of the nitride material 224 that are removed may then be back filled with a conductive material 226, forming the SMOI structure 250 shown in FIG. 38. Replacing the nitride material 224 with the conductive material 226 may be used to form an SMOI structure 250 having multiple layers of the conductive material 226, which is buried. While the layers of the conductive material 226 are shown as having equal thicknesses, it is understood that different layers of the conductive material 226 may have varying thicknesses depending on the desired use of the SMOI structure 250. The multiple layers of the conductive material 226 may be used to form multiple interconnects, such as word lines and bit lines. In additional embodiments, when forming a semiconductor device on/in the second semiconductor substrate 202', only the uppermost portion of the conductive material 226 may be utilized to form a semiconductor device as described in greater detail below, and the lower portions of conductive material 226 may remain intact. The lower

portions of conductive material 226 that remain intact may help improve the bond strength and stability of the SMOI structure 250.

The SMOI structures 30, 50, 70, 90, 120, 140, 170, 200, 250 described herein may be utilized to form numerous semiconductor devices as known in the art including those described in U.S. Patent No. 7,589,995 to Tang et al. entitled *One-transistor Memory Cell with Bias Gate*, U.S. Patent Application Publication No. 2007/0264771 to Ananthan et al. entitled *Dual Work Function Recessed Access Device and Methods of Forming*, U.S. Patent Application No. 12/410,207 to Tang et al. entitled *Methods, Devices, and Systems Relating to Memory Cells Having a Floating Body*, U.S. Patent Application No. 12/419,658 to Tang
 10 entitled *Methods, Devices, and Systems Relating to Memory Cells Having a Floating Body*. The disclosure of each of the foregoing documents is incorporated herein in its entirety by this reference. The SMOI structures 30, 50, 70, 90, 120, 140, 170, 200, 250 may be used to form any semiconductor device with two or more terminals. For example, the SMOI structures 30, 50, 70, 90, 120, 140, 170, 200, 250 may be used to form dynamic random
 15 access memory (DRAM), resistive, non-volatile RAM (ReRAM), phase change RAM (PCRAM), one-time programmable read-only memory (OTP ROM), or cache memory devices.

FIG. 39 illustrates one example of an embodiment of a semiconductor device 300 including an SMOI structure 301 having a conductive material 304 buried beneath a second
 20 semiconductor substrate 312. The SMOI structure 301 may include, for example, a first semiconductor substrate 306, an insulator material 308, an amorphous silicon material 310, the conductive material 304, and the second semiconductor substrate 312. The SMOI structure 301 may be formed in a manner analogous to that described above in regard to FIGs. 1-6, 7-10, 11-14, 15-18, 19-21, 22-28, 32-34, or 35-38.

The amorphous silicon material 310, the conductive material 304, and the second
 25 semiconductor substrate 312 may be patterned by conventional techniques in a first direction to form bit lines 314. Alternatively, if the SMOI structure 301 is formed in a manner analogous to that described above in regard to FIGs. 22-28, the conductive material 304 may already be patterned in the first direction. The second semiconductor substrate 312 may be
 30 patterned by conventional techniques in a second direction perpendicular to the first direction to form pillars 316 above the bit lines 314. The pillars 316 may be doped, as known in the

art, to form a drain region 318, a source region 320, and a channel region 322. Alternatively, the second semiconductor substrate 312 may already be doped as previously described regarding FIGs. 11-14 and 15-18. Since the drain region 318, the source region 320, and the channel region 322 are formed vertically from the body of the pillars 316 and the pillar 316 is directly on top of the bit line 314, a higher device density may be achieved than with a conventional plan arrangement. A gate dielectric 324 may be formed on the sidewalls of the pillars 316 adjacent the channel regions 322. A gate 326 may also be formed on the sidewalls of the pillars 316 adjacent the gate dielectric 324. The gate dielectric 324 and the gate 326 may be formed using conventional techniques including conventional spacer etch techniques, which are not described in detail herein.

By utilizing the SMOI structure 301 to form the semiconductor device 300, the semiconductor device 300 may be formed in as few as three patterning acts. As previously described, the second semiconductor substrate 312 may be patterned in a first direction to form bit lines 314, the second semiconductor substrate 312 may be patterned in a second direction to form pillars 316 above the bit lines, and the gate 326 and the gate dielectric 324 may be patterned to form gate 326 and the gate dielectric 324 on the sidewalls of the pillars 316. Additionally, because the drain region 318, the source region 320, and the channel region 322 are formed from the pillar 316 above the bit line 314, no separate contact is needed to electrically connect the bit line 314 and the drain region 318. Furthermore, because a logic device (not shown) and back end of the line (BEOL) elements (not shown) may be formed on the first semiconductor substrate 306 prior to forming the semiconductor device 300, the semiconductor device 300 is not exposed to the processing conditions for forming the logic device and the BEOL elements. Avoiding exposure to such processing conditions may improve the reliability of the semiconductor device 300.

FIG. 40 illustrates another embodiment of a semiconductor device 400 including an SMOI structure 401 having a conductive material 403 buried beneath a second semiconductor substrate 412. The semiconductor device 400 may include a memory cell coupled to an access device, such as a diode 422. The SMOI structure 401 may include, for example, a first semiconductor substrate 406, a dielectric material 408, an amorphous silicon material 409, the conductive material 403, and the second semiconductor substrate 412. The SMOI

structure 401 may be formed in a manner analogous to that described above in regard to FIGs. 1-6, 7-10, 11-14, 15-18, 19-21, 22-28, 32-34, or 35-38.

The amorphous silicon material 409, the conductive material 403, and the second semiconductor substrate 412 may be patterned by conventional techniques in a first direction to form word lines 415. Alternatively, if the SMOI structure 401 is formed in a manner analogous to that described above in regard to FIGs. 22-28, the conductive material 403 may already be patterned in the first direction. A portion of the second semiconductor substrate 412 may be patterned in a second direction by conventional techniques to form a pillar 423. The second semiconductor substrate 412 may be doped by conventional techniques to form the diode 422 over the word lines 415. For example, the second semiconductor substrate 412 may be formed of a single crystalline silicon material and may be doped to form an N doped silicon material 414 and a P doped silicon material 416. The N doped silicon material 414 may include a portion of the second semiconductor substrate 412 extending over the word lines 415 which is not etched in the second direction. The P doped silicon material 416 may include the portion of the second semiconductor substrate 412 etched in the second direction to form the pillar 423. Alternatively, the second semiconductor substrate may already be doped as previously described regarding FIGs. 11-14 and 15-18. A bottom electrode 418 for the memory device 400 may be formed over the diode 412 using conventional techniques. For example, in one embodiment, the material of the bottom electrode 418 may be deposited over the second semiconductor substrate 412 prior to patterning the second semiconductor substrate 412. The material of the bottom electrode 418 may then be patterned and etched, using conventional techniques, simultaneously with the patterning and etching of the second semiconductor substrate 412. A memory medium 420, and a terminal electrode or bit line 424 may be formed over the diode 422 and in electrical communication therewith, using conventional techniques, which are not described in detail herein.

By utilizing the SMOI structure 401 to form the semiconductor device 400, the semiconductor device 400 may be formed in as few as three patterning acts. As previously described, the amorphous silicon material 409, the conductive material 403, and the second semiconductor substrate 412 may be patterned in a first direction to form word lines 415; the second semiconductor substrate 412 and the bottom electrode 418 may be patterned in a second direction to form the diode 422 and the bottom electrode 418; and the memory

medium 420 and the bit line 424 may be patterned to form the memory medium 420 and the bit line 424 above the diodes 422. Because the memory medium 420 is one of the last materials to be deposited, phase change or resistant change materials may be used as the memory medium 420 since the memory medium 420 may not be exposed to, and altered by, high processing temperatures.

FIG. 41 illustrates another embodiment of a semiconductor device 500 including an SMOI structure 502 having a conductive material 504 buried beneath a second semiconductor substrate 514. The semiconductor device 500 may include a floating body memory cell 501 formed over and/or within the SMOI structure 502. The SMOI structure 502 may include, for example, a first semiconductor substrate 506, an insulator material 508, an amorphous silicon material 510, the conductive material 504, a high-k gate dielectric material 512, and the second semiconductor substrate 514. The SMOI structure 502 may be formed in a manner analogous to that described above in regard to FIGs. 29-31.

The floating body memory cell 501 includes an active region 516 surrounded on the sides by an additional insulator material 518. The active region 516 may be formed from the monocrystalline silicon of the second silicon substrate 514. The entire thickness of the second silicon substrate 514 may be used to form the floating body memory cell 501 as shown in FIG. 33, the underlying high-k gate dielectric material 512 forming a back gate-dielectric and the conductive material 504 forming a metal back gate. Source and drain regions 526 may be formed by doping portions of the active region 516. The source and drain regions 526 will be doped differently than the active region 516. For example, the active region 516 may include P doped silicon while the source and drain regions 526 include N doped silicon.

As shown in FIG. 41, a second high-k material for a gate dielectric 520 is formed on the active region 516. The material for high-k gate dielectric 520 has a dielectric constant that is greater than that of silicon dioxide. Examples of a suitable material for high-k gate dielectric 520 include hafnium silicate, zirconium silicate, hafnium dioxide, or zirconium dioxide. A field-effect transistor (FET) gate 522 is formed on the high-k gate dielectric 520. The FET gate 522 and underlying high-k gate dielectric 520 may then be defined using conventional photolithographic techniques in combination with suitable etch processes, as

known in the art. Spacers 524 may be formed flanking the sides of the FET gate 522 using conventional techniques, which are not described in detail herein.

By utilizing the SMOI structure 502 to form the semiconductor device 500, the floating body memory cell 501 may be formed in electrical communication with the conductive material 504, thus eliminating the need for an additional electrical contact between the floating body memory cell 501 and the conductive material 504. Additionally, because a logic device (not shown) and back end of the line (BEOL) elements (not shown) may be formed on the first semiconductor substrate 506 prior to forming floating body memory cell 501, the floating body memory cell 501 is not exposed to the processing conditions used to form the logic device and the BEOL elements. Avoiding exposure to such processing conditions may improve the reliability of the semiconductor device 500.

FIG. 42 illustrates another embodiment of a semiconductor device 600 including an SMOI structure 601 having a conductive material 603 buried beneath a second semiconductor substrate 614. The SMOI structure 601 may include, for example, a first semiconductor substrate 605, an insulator material 607, an amorphous silicon material 609, the conductive material 603, a dielectric material 611 and a second semiconductor substrate 614. The SMOI structure 601 may be formed in a manner analogous to that described above in regard to FIGs. 29-31.

The second semiconductor substrate 614 may be patterned and doped, as known in the art, to form a floating body region 616, a drain region 618 and a source region 619. The second semiconductor substrate 614 may be further patterned to form a recess in the floating body region 616 between the drain region 618 and the source region 619. A word line 620 may be formed in the recess. A dielectric material 622 may be formed between the word line 620 and the floating body region 616. The buried conductive material 603 acts as a buried gate for the memory cell. A contact 624 may be formed above the drain region 618 leading to a bit line 626. The contact 624 may comprise, for example, a N⁺ doped polysilicon plug or a metal plug. A common source 628 may be formed above the source region 619.

Fig. 43 illustrates a semiconductor device 700 including a plurality of the semiconductor devices 600 (FIG. 42). As illustrated in FIG. 43, the amorphous silicon material 609, the conductive material 603 and the dielectric material 611 may also be etched to form rows which are parallel to the bit lines 626. Similarly, in additional embodiments,

the amorphous silicon material 609, the conductive material 603 and the dielectric material 611 may be etched to form rows (not shown) which are parallel to the bit lines 626.

By utilizing the SMOI structure 601 to form the semiconductor device 700, the floating body region 616 may be formed on top of the conductive material 603, thus
5 eliminating the need for an additional electrical contact between the floating body region 616 and the conductive material 603. Additionally, because a logic device (not shown) and back end of the line (BEOL) elements (not shown) may be formed on the first semiconductor substrate 605 prior to forming floating body region 616, the floating body region 616 is not exposed to the processing conditions used for forming the logic device and the BEOL
10 elements. Avoiding exposure of the floating body region 616 to such processing conditions may improve the reliability of the semiconductor device 600.

Semiconductor devices, such as those previously described herein, may be used in embodiments of electronic systems of the present invention. For example, FIG. 44 is a schematic block diagram of an illustrative electronic system 800 according to the present
15 invention. The electronic system 800 may comprise, for example, a computer or computer hardware component, a server or other networking hardware component, a cellular telephone, a digital camera, a personal digital assistant (PDAs), portable media (e.g., music) player, etc. The electronic system 800 includes at least one memory device 801. The electronic system 800 further may include at least one electronic signal processor device 802 (often referred to
20 as a "microprocessor"). At least one of the electronic signal processor device 802 and the at least one memory device 801 may comprise, for example, an embodiment of the semiconductor device 300, 400, 500, 600, 700 described above. In other words, at least one of the electronic signal processor device 802 and the at least one memory device 801 may comprise an embodiment of a semiconductor device including an SMOI structure having a
25 buried conductive material as previously described in relation to the semiconductor devices 300, 400, 500, 600, 700 shown in FIGs. 39-43. The electronic system 800 may further include one or more input devices 804 for inputting information into the electronic system 800 by a user, such as, for example, a mouse or other pointing device, a keyboard, a touchpad, a button, or a control panel. The electronic system 800 may further include one or
30 more output devices 806 for outputting information (e.g., visual or audio output) to a user such as, for example, a monitor, a display, a printer, an audio output jack, a speaker, etc. In

some embodiments, the input device 804 and the output device 806 may comprise a single touchscreen device that can be used both to input information to the electronic system 800 and to output visual information to a user. The one or more input devices 804 and output devices 806 may communicate electrically with at least one of the memory device 801 and
5 the electronic signal processor device 802.

CONCLUSION

In some embodiments, the present invention includes semiconductor-metal-on-insulator (SMOI) structures, devices including such structures and methods for forming such
10 structures. The SMOI structures may include an insulator material on a first semiconductor substrate, an amorphous silicon material bonded to the insulator material, a conductive material over the amorphous silicon material and a second semiconductor substrate over the conductive material. A dielectric material may also be disposed between the conductive material and the second semiconductor substrate. In other embodiments, the conductive
15 material may be patterned and adjacent portions of the patterned conductive material may be separated from one another by a dielectric material.

In additional embodiments, the present invention includes an SMOI that includes an insulator material on a first semiconductor substrate, an amorphous germanium material bonded to the insulator material, a conductive material over the amorphous germanium
20 material and a second semiconductor substrate over the conductive material.

In additional embodiments, the present invention includes an SMOI structure that includes an insulator material on a first semiconductor substrate, a conductive material over the insulator material, at least one portion of an epitaxial silicon material and at least one portion of a silicon-germanium material, the at least one portion of the epitaxial silicon
25 material or the at least one portion of the silicon-germanium material bonded to the insulator material, and a second semiconductor substrate over the conductive material. The insulator material may be formed of an oxide material having an amorphous silicon material formed thereon.

In additional embodiments, the present invention includes an SMOI structure
30 including a first semiconductor substrate, at least one portion of an oxide material and at least

one portion of a conductive material formed over the first semiconductor substrate, and a second semiconductor substrate formed over the conductive material.

In yet further embodiments, the present invention includes a semiconductor device that includes an insulator material on a first semiconductor substrate, an amorphous silicon material bonded to the insulator material, a conductive material over the amorphous silicon material, a second semiconductor substrate over the conductive material, and a memory cell on the second silicon substrate. The conductive material may form an interconnect. A logic device may also be formed on the first semiconductor substrate. In some embodiments, a dielectric material may be disposed between the conductive material and the second semiconductor substrate. The memory cell of the semiconductor device may include a floating body memory cell which includes an active area substantially physically isolated by an insulating material, a drain region and a source region formed within the active area, a high-k dielectric material formed on an active area between the drain region and the source region and a metal gate formed on the high-k dielectric.

In yet further embodiments, the present invention includes methods of forming an SMOI structure that include forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate, forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous silicon material over the conductive material, and an implanted zone within the precursor semiconductor substrate, bonding the amorphous silicon material of the donor wafer to the insulator material of the acceptor wafer, and removing a portion of the precursor semiconductor substrate proximate the implanted zone within the precursor semiconductor substrate. In some embodiments, at least one surface of the amorphous silicon material and a surface of the insulator material may be treated with a chemical, a plasma, or an implant activation before bonding the amorphous silicon material of the donor wafer to the insulator material.

In yet further embodiments, the present invention includes a method of fabricating a semiconductor device including forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate, forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous silicon material over the conductive material, and an implanted zone within the precursor semiconductor substrate, bonding the amorphous silicon material of the donor wafer to the insulator material of the

acceptor wafer, removing a portion of the precursor semiconductor substrate proximate the implanted zone to form a second semiconductor substrate, and fabricating at least one memory cell on the second semiconductor substrate.

5 In yet further embodiments, the present invention includes methods of forming an SMOI structure that include forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate, forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous germanium material over the conductive material, and an implanted zone within the precursor semiconductor substrate, bonding the amorphous germanium material of the donor wafer to the insulator material of
10 the acceptor wafer, and removing a portion of the precursor semiconductor substrate proximate the implanted zone within the precursor semiconductor substrate.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, the invention is not intended to be limited to the
15 particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the scope of the invention as defined by the following appended claims and their legal equivalents.

CLAIMS

What is claimed is:

1. A semiconductor-metal-on-insulator structure comprising:

5 an insulator material on a first semiconductor substrate;

an amorphous silicon material bonded to the insulator material;

a conductive material over the amorphous silicon material;

a second semiconductor substrate over the conductive material; and

a dielectric material disposed between the conductive material and the

10 second semiconductor substrate.

2. The semiconductor-metal-on-insulator structure of claim 1, wherein the
15 conductive material is patterned and adjacent portions of the patterned conductive material
are separated from one another by a dielectric material.

3. The semiconductor-metal-on-insulator structure of claim 1, wherein the
conductive material comprises a conductive silicide material.

20 4. A semiconductor-metal-on-insulator structure comprising:

an insulator material on a first semiconductor substrate;

an amorphous germanium material bonded to the insulator material;
a conductive material over the amorphous germanium material; and
a second semiconductor substrate over the conductive material.

5 5. A semiconductor-metal-on-insulator structure comprising:

an insulator material on a first semiconductor substrate;
a conductive material over the insulator material;
an amorphous silicon material over the conductive material; and
a second semiconductor substrate over the conductive material.

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6. The semiconductor-metal-on-insulator structure of claim 5, further comprising
a bonding material disposed between the conductive material and the amorphous silicon
material.

15 7. The semiconductor-metal-on-insulator structure of claim 6, wherein the
bonding material comprises at least one of an additional amorphous silicon material and an
oxide material.

8. A semiconductor-metal-on-insulator structure comprising:
20 an insulator material on a first semiconductor substrate;
a conductive material over the insulator material;

at least one portion of an epitaxial silicon material and at least one portion of a silicon-germanium material, the at least one portion of the epitaxial silicon material or the at least one portion of the silicon-germanium material bonded to the insulator material; and

5 a second semiconductor substrate over the conductive material.

9. The semiconductor-metal-on-insulator structure of claim 8, wherein the insulator material comprises an oxide material having an amorphous silicon material formed thereon.

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10. A semiconductor-metal-on-insulator structure comprising:

a first semiconductor substrate;

at least one portion of an oxide material and at least one portion of a conductive material

formed over the first semiconductor substrate; and

15 a second semiconductor substrate formed over the conductive material.

11. A semiconductor device comprising:

an insulator material on a first semiconductor substrate;

an amorphous silicon material bonded to the insulator material;

20 a conductive material over the amorphous silicon material;

a second semiconductor substrate over the conductive material; and

a memory cell on the second semiconductor substrate.

12. The semiconductor device of claim 11, wherein the conductive material forms an interconnect.

5 13. The semiconductor device of claim 11, further comprising a logic device formed on the first semiconductor substrate.

14. The semiconductor device of claim 11, further comprising a dielectric material disposed between the conductive material and the second semiconductor substrate.

10

15. The semiconductor device of claim 14, wherein the memory cell comprises a floating body memory cell comprising:

an active area substantially physically isolated by an insulating material;

a drain region and a source region formed within the active area;

15 a high-k dielectric material formed on the active area between the drain region and the source region; and

a metal gate formed on the high-k dielectric.

16. A method for fabricating a semiconductor-metal-on-insulator structure,
20 comprising:

forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate;

forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous silicon material over the conductive material, and an implanted zone within the precursor semiconductor substrate;

5 bonding the amorphous silicon material of the donor wafer to the insulator material of the acceptor wafer; and

removing a portion of the precursor semiconductor substrate proximate the implanted zone within the precursor semiconductor substrate.

17. The method of claim 16, further comprising treating at least one of a surface of the amorphous silicon material and a surface of the insulator material with a chemical, a plasma, or an implant activation before bonding the amorphous silicon material of the donor wafer to the insulator material of the acceptor wafer.

18. The method of claim 16, wherein forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate comprises forming an oxide material over a first semiconductor substrate comprising crystalline silicon.

19. The method of claim 16, wherein forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous silicon material over the conductive material, and an implanted zone within the precursor semiconductor substrate comprises forming a conductive material over a crystalline silicon substrate, an amorphous silicon material over the conductive material, and a hydrogen-implanted zone within the crystalline silicon substrate.

20. The method of claim 16, wherein forming a donor wafer further comprises forming a dielectric material between the conductive material and the precursor semiconductor substrate.

21. The method of claim 16, wherein forming a donor wafer comprising a conductive material over a precursor semiconductor substrate comprises forming a non-reactive conductive material over the precursor semiconductor substrate and a reactive
5 conductive material over the non-reactive conductive material and reacting the reactive conductive material with the amorphous silicon material of the donor wafer to form a conductive silicide material.

22. The method of claim 16, wherein forming the conductive material over the
10 precursor semiconductor substrate comprises:

depositing the conductive material over the precursor semiconductor substrate;

forming a cap material over the conductive material;

patterning the cap material and the conductive material; and

forming a dielectric material between adjacent portions of the patterned cap material and
15 patterned conductive material.

23. The method of claim 16, wherein forming the donor wafer further comprises forming at least one portion of an epitaxial silicon material and at least one portion of a silicon-germanium material between the conductive material and the amorphous silicon
20 material.

24. The method of claim 16, wherein forming the donor wafer further comprises forming at least one portion of an oxide material and at least one portion of a nitride material between the conductive material and the amorphous silicon material.

25. A method of fabricating a semiconductor device, comprising:

forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate;

5 forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous silicon material over the conductive material, and an implanted zone within the precursor semiconductor substrate;

bonding the amorphous silicon material of the donor wafer to the insulator material of the acceptor wafer;

10 removing a portion of the precursor semiconductor substrate proximate the implanted zone to form a second semiconductor substrate; and

fabricating at least one memory cell on the second semiconductor substrate.

26. The method of claim 25, further comprising patterning the conductive material

15 to form at least one of a buried word line and a buried bit line.

27. The method of claim 25, wherein fabricating at least one memory cell on the second semiconductor substrate comprises:

forming an active area from a portion of the second semiconductor substrate substantially
20 surrounded on the sides and bottom by an additional insulator material;

forming a high-k gate dielectric and a metal gate on the active area; and

forming a source region and a drain region in the active area.

28. The method of claim 25, wherein fabricating at least one memory cell on the second semiconductor substrate comprises:

etching the second semiconductor substrate to form at least one pillar;

forming a source region, an active area, and a drain region in the at least one pillar; and

5 forming a gate dielectric and a gate on the active area.

29. The method of claim 25, wherein fabricating at least one memory cell on the second semiconductor substrate comprises:

forming a diode in the second semiconductor substrate; and

10 forming a bottom electrode, a memory medium, and a top electrode on the diode.

30. A method for fabricating a semiconductor-metal-on-insulator structure, comprising:

forming an acceptor wafer comprising an insulator material formed over a first semiconductor substrate;

15 forming a donor wafer comprising a conductive material over a precursor semiconductor substrate, an amorphous germanium material over the conductive material, and an implanted zone within the precursor semiconductor substrate;

bonding the amorphous germanium material of the donor wafer to the insulator material of the acceptor wafer; and

20 removing a portion of the precursor semiconductor substrate proximate the implanted zone within the precursor semiconductor substrate.