

Description

The invention relates to an integrated circuit with a switching device comprising, connected between two supply lines, a series arrangement of conduction channels of a first and second transistor respectively, said transistors being of mutually opposite conductivity type, receiving the same input voltage at their respective control terminals and generating an output voltage at the common node between said transistors, the device comprising at least one additional conduction channel, in parallel to one of the conduction channels of the first and second transistor, the device comprising control means responsive to the output voltage, for causing the additional conduction channel to conduct when the device switches to make the transistor conductive in parallel to which the additional transition channel is placed.

Such an integrated circuit is known from US Patent No. 4,498,021. According to this publication, the additional current path serves to boost the speed with which the output voltage of the device switches state, by providing additional current to charge any load capacitance of the device.

Another such circuit, which also serves to boost the speed is known from US patent No. 4,532,436. In both circuits the additional conduction channels is turned off as soon as the output voltage of the series arrangement has switch.

Various problems arise when a fast semiconductor integrated circuit (IC) interacts with the outside world. One problem is that the voltages on the internal supply lines often "bounce" up and down. The bounce can cause the IC to operate improperly when it responds to an input signal having a slowly changing voltage. The problem normally becomes more serious as the IC speed increases.

In explanation of supply line bounce, Fig. 1 illustrates a portion of a digital IC 10 that receives largely constant external supply voltages V_{HH} and V_{LL} at respective externally accessible supply terminal (or pads) T_H and T_L . V_{HH} is greater than V_{LL} . IC 10 produces a circuit output voltage V_O at an externally accessible output terminal T_O in response to a circuit input voltage V_I received at an externally accessible input terminal T_I . A capacitor C_O , which may be real or parasitic, is connected between terminal T_O and the V_{LL} supply.

The illustrated portion of IC 10 is a conventional inverting driver powered by high and low internal supply voltages V_H and V_L provided on lines connected respectively to terminals T_H and T_L . Responsive to an internal input voltage V_A supplied on a line connected to terminal T_I , the driver produces an internal output voltage V_D on a line connected to terminal T_O . Parasitic inductances L_L , L_H , L_I and L_O are respectively associated with the lines carrying voltages V_L , V_H , V_A and V_D .

The driver consists of an input inverter 12, an intermediate inverter 14, and an output inverter 16, each of which is progressively larger so as to provide progressively more current. Inverter 12 is formed with complementary input field-effect transistors (FET's) $Q1_N$ and $Q1_P$ whose gates receive voltage V_A and whose interconnected drains provide an inverter output voltage V_B logically inverse to voltage V_A . Inverter 14, which is typically configured the same as inverter 12, generates a voltage V_C inverse to voltage V_B . Inverter 16 consists of complementary output FET's $Q2_N$ and $Q2_P$ whose gates receive voltage V_C and whose interconnected drains provide voltage V_D as the inverse of voltage V_C . FET's $Q1_N$ and $Q2_N$ are N-channel devices whose sources are connected to the V_L supply line. FET's $Q1_P$ and $Q2_P$ are P-channel transistors having their sources tied to the V_H supply line.

Returning to inverter 12, it changes state as the voltage difference $V_A - V_L$ passes an inverter threshold voltage V_T . Threshold V_T is at a nominal value V_S when internal supply voltages V_L and V_H are respectively at (or very close to) V_{LL} and V_{HH} . Accordingly, inverter 12 switches from a high logic state to a low logic state as voltage V_A rises above $V_{LL} + V_S$. This is manifested in voltage V_B which goes from a high voltage level close to V_{HH} to a low voltage level close to V_{LL} . When V_A later drops below $V_{LL} + V_S$, inverter 12 switches from its low logic state to its high logic state. V_B then rises from V_{LL} back up to V_{HH} .

Consider what happens if input V_I changes very slowly. With reference to Fig. 2 which roughly shows how certain voltages vary with time for IC 10, assume that V_I is initially low. Also assume that V_L and V_H are respectively at V_{LL} and V_{HH} . V_A is then low, causing V_B to be at V_{HH} . V_C is low so that FET $Q2_N$ is turned off and FET $Q2_P$ is turned on. V_D and V_O are both at V_{HH} . Capacitor C_O is charged to a high level.

As V_I rises slowly, V_A tracks V_I closely. Inductance L_I does not have any significant effect on V_A . At the time t_1 , V_A starts to go above $V_{LL} + V_S$. This causes V_B to drop rapidly to V_{LL} . V_C goes high to turn FET $Q2_N$ on and FET $Q2_P$ off. V_D drops rapidly to V_{LL} . At a time t_2 depending on the transmission delays through inverters 14 and 16, capacitor C_O starts discharging to the V_{LL} supply by way of a path through elements L_O , $Q2_N$ and L_L to pull V_O rapidly down to V_{LL} .

The current flowing through this path varies with time in a non-linear manner. Since the voltage across an inductor is the inductance times the time rate of change of current flowing through the inductor, a positive voltage builds up across inductance L_L , reaching a maximum, at a time t_3 . A positive (or upward going) spike in V_L thereby occurs at t_3 as shown in Fig. 2. The V_L spike at t_3 is the "first" spike in a set of timewise contiguous pairs of alternating spikes that die out quickly, of which only the first pair of alternating spikes are actually shown in Fig. 2. The same applies to the further supply line spikes discussed below for

Fig. 2 and to the supply line spikes illustrated in the other time diagrams herein.

The V_L spike at t_3 is often so high that $V_A - V_L$ temporarily drops below threshold V_T . This is true even though the attendant reduction of the difference between V_H and V_L during the positive V_L spike reduces V_T somewhat. See shaded area 18 in Fig. 2. (Note that the comparison of V_L to $V_A - V_T$ shown in the various time diagrams herein is equivalent to the comparison of $V_A - V_L$ to V_T which is more difficult to illustrate graphically). Inverter 12 then makes a pair of rapid changes in logic state at approximately a time t_4 , causing V_B to spike upwards. In turn, the V_B spike causes a positive V_0 spike to occur at a time t_5 . Even if the C_0 discharge current flowing through FET Q2N in output inverter 16 were not sufficient in itself to cause the V_0 spike, it could be produced as the result of several such output inverters acting in unison in IC 10.

The rapid charging and discharging of capacitor C_0 that occur with the V_0 spike produce a negative (or downward going) V_H spike followed by another positive V_L spike. In the example shown in Fig. 2, neither of the further spikes is sufficient to cause $V_A - V_L$ to fall below V_T . However, if V_L were rising slower than indicated, the further supply line bounce could cause inverter 12 to make additional undesired transitions, thereby resulting in further V_0 spiking.

The same situation arises if V_L drops slowly, except that the polarities and supply lines are reversed. The first spike is a negative V_H spike that results from the rapid charging of capacitor C_0 by way of a path through elements L_H , Q2P and L_0 .

The V_0 spikes and the corresponding spikes in V_B , V_C and V_D can be disastrous. They can cause a circuit (such as a flip-flop) responsive to V_0 , V_B , V_C or V_D to be set in a wrong state.

To overcome the bounce problem, one might consider replacing inverter 12 with a device (such as a Schmitt trigger) having a pair of separate static voltage thresholds. While static hysteresis might be useful in certain applications, it is not effective if the two thresholds must lie within a narrow voltage range. A solution that entails a single static threshold is desirable.

A better solution is to utilize dynamic hysteresis to prevent internal supply line voltage bounce from causing unwanted changes in state. The present hysteresis is termed "dynamic" because a change in device threshold voltage triggered by a change in logic state occurs only for a prescribed period of time. When that period expires, the threshold voltage automatically returns to its original value. The device therefore has only one static threshold. This is especially useful in a high-speed IC having a narrow threshold range in which the input voltage must switch. This also avoids the additional propagation delays that normally occur with static hysteresis.

A circuit with dynamic hysteresis is known from U.S. Patent 3,718,864 (Kelly). This prior art circuit functions as a cross-over detector. The known circuit includes a comparator for comparing an input voltage at an input terminal with a reference voltage at a reference terminal. The comparator is biased at the reference terminal through a resistance connected to a supply voltage terminal. The comparator's output is coupled to the reference terminal via a capacitance, thus establishing an a.c. feedback-path. Consequently, in response to an output voltage change the reference voltage experiences an associated pulse-like change.

However, this prior art circuit does not mention the bounce problem in digital circuits and it does not teach how dynamic hysteresis can be realized in digital circuits which use inverter circuits built of complementarily controlled transistors whose conduction paths are in series arrangement.

It is an object of the invention to provide an integrated digital circuit which overcomes the bounce problem.

The integrated circuit according to the invention is characterized in that the control terminals of the first and second transistor are interconnected with an externally accessible terminal of the integrated circuit, and in that the control means are arranged for causing the additional conduction channel to conduct only for a prescribed period of time after the output voltage of the device has changed logic state.

An embodiment of the invention is characterized in that the at least one additional current conduction channel is part of a further transistor having the same conductivity type as the transistor in parallel to which its conduction channel is placed, the further transistor receiving on its control terminal a control voltage generated by said control means.

The first and second transistor are typically an N-channel and a P-channel FET respectively, having their gates responsive to voltage V_A , sources respectively coupled to the lines carrying voltage V_L and V_H and drains coupled together to provide an output voltage V_B inverse to voltage V_A . The further transistor is typically an N-channel FET having its gate responsive to signals from the control circuit, its source coupled to V_L line and drain coupled to the drain of the first transistor. A further P-channel FET may also be provided having its gate responsive to signals from the control circuit, its source coupled to the V_H line and drain coupled to the drain of the second transistor.

More particularly, the present device is incorporated in an electronic circuit in which a low supply voltage V_L and a high supply voltage V_H are provided to power the device. In response to an input voltage V_A , the device changes state as $V_A - V_L$ passes a threshold voltage V_T . With threshold V_T substantially at a value V_S and with voltages V_L and V_H substantially at re-

spective values V_{LL} and V_{HH} , the device switches from a first state to a second state as V_A rises above $V_{LL}+V_S$ and from the second state to the first state as V_A drops below $V_{LL}+V_S$.

The device includes a dynamic hysteresis circuit that, after V_A rises above $V_{LL}+V_S$, temporarily decreases V_T below that which would otherwise be present and/or, after V_A drops below $V_{LL}+V_S$, temporarily increases V_T above what would otherwise be present. V_T normally returns to V_S before V_A starts moving in the direction opposite to that in which it was moving when V_T changed.

An embodiment of the invention is characterized in that the first and second current conduction paths comprise a conduction channel of a first and second transistor, respectively, said transistors being of a mutually complementary conductivity type, and receiving the same input voltage at their respective control terminals, whereby the at least one additional current conduction path comprises a conduction channel of a further transistor having the same conductivity type as the transistor in parallel to which its conduction channel is placed, the further transistor receiving on its control terminal a control voltage generated by said control means.

The first and second transistor are typically an N-channel and a P-channel FET respectively, having their gates responsive to voltage V_A , sources respectively coupled to the lines carrying voltages V_L and V_H and drains coupled together to provide an output voltage V_B inverse to voltage V_A . The further transistor is typically an N-channel FET having its gate responsive to signals from the control circuit, its source coupled to the V_L line and drain coupled to the drain of the first transistor. A further P-channel FET may also be provided having its gate to signals from the control circuit, its source coupled to the V_H line and drain coupled to the drain of the second transistor.

The control circuit causes the further N-channel FET to turn on temporarily in response to voltage V_B going from a high level to a low level. This temporarily increases the width of the pertinent conducting N-channel area in the device so as to reduce V_T until the further N-channel FET turns off. Likewise, the control circuit causes the further P-channel FET to turn on temporarily in response to voltage V_B going from its low level to its high level. The width of the pertinent conducting P-channel area in the device thereby increases to raise V_T briefly.

The temporary change in V_T provides a clearance that prevents the present device from making a pair of rapid changes of state as a result of internal supply line bounce when V_A is changing slowly. This avoids output voltage spikes.

BRIEF DESCRIPTION OF THE DRAWINGS.

Fig.1 is a circuit diagram for a portion of a digital

IC utilizing a conventional input inverter.

Fig. 2 is a pair of graphs for various voltages as a function of time for the IC of Fig. 1.

Fig. 3 is a circuit diagram for a portion of a digital IC that utilizes an input inverting device having dynamic hysteresis according to the invention.

Figs. 4a and 4b are two pairs of graphs for various voltages as a function of time for the IC of Fig. 3.

Figs. 5 and 6 are circuit diagrams for specific embodiments of the control circuit 26 in Fig. 3.

Like reference symbols are employed in the drawings and in the description of the preferred embodiments to represent the same or very similar item or items. In the drawings, each N-channel FET has an arrow pointing towards its channel. Each P-channel FET has an arrow pointing away from its channel. All of the FET's shown in the drawings are enhancement-mode insulated-gate devices.

DESCRIPTION OF THE PREFERRED EMBODIMENTS.

Referring to the drawings, Fig. 3 illustrates a portion of a digital IC 20 in which a very fast logic circuit powered by high and low internal supply voltages V_H and V_L operates on input voltage V_A and possibly on other input voltages (not shown) to produce output voltage V_D . The logic circuit contains an input inverting device 22 that produces voltage V_B as the logical inverse of voltage V_A . Device 22 is formed with input inverter 12 consisting of FET's $Q1_N$ and $Q1_P$ arranged as described above and a circuit 24 that provides dynamic hysteresis for the threshold voltage V_T of device 22.

Dynamic hysteresis circuit 24 consists of a control circuit 26 powered by supply voltages V_H and V_L , an N-channel FET $Q3_N$, and a P-channel FET $Q3_P$. In response to voltage V_B , control circuit 26 supplies threshold-control voltages V_N and V_P to the respective gates of FET's $Q3_N$ and $Q3_P$. Their sources are respectively connected to the V_L and V_H supply lines, while their drains are connected to the drains of FET's $Q1_N$ and $Q1_P$ to produce voltage V_B . FET $Q3_N$ is therefore "in parallel" with FET $Q1_N$. Likewise FET's $Q3_P$ and $Q1_P$ are in parallel.

The threshold voltage for an inverter formed with complementary FET's depends on the ratio $R_{P/N}$ of the P-channel width to the N-channel width (at constant channel length). This means the widths of the channel areas that are conducting at the threshold point. The threshold voltage increases when $R_{P/N}$ increases and vice versa.

FET's $Q3_N$ and $Q3_P$ are normally off or at so low conductive levels as to be effectively off. Accordingly, the quiescent value of $R_{P/N}$ for device 22 is simply the $Q1_P$ channel width divided by the $Q1_N$ channel width since FET's $Q1_N$ and $Q1_P$ are both conducting at the threshold point, one in the midst of turning on and the

other in the midst of turning off. If FET Q3_N is on but FET Q3_P is off, the N-channel width for device 22 increases since FET's Q3_N and Q1_N are in parallel. R_{P/N} for device 22 is therefore less than its quiescent value. In like manner, R_{P/N} for device 22 is greater than the quiescent value when FET Q3_P is on but FET Q3_N is off.

With the foregoing in mind, device 22 operates as follows. FET's Q3_N and Q3_P are initially off. Supply voltages V_L and V_H are initially at (or very near) respective substantially constant levels V_{LL} and V_{HH}. Under these conditions, threshold V_T is at quiescent value V_S determined by the quiescent R_{P/N} of device 22. When V_A-V_L passes V_T, device 22 changes state.

If V_A rises above V_{LL}+V_S, FET Q1_N turns on and FET Q1_P turns off. Device 22 as manifested by the conductive conditions of FET's Q1_N and Q1_P switches from a high logic state to a low logic state, causing voltage V_B to go from a high level near V_{HH} to a low level near V_{LL}. Responsive to this change in voltage V_B, control circuit 26 temporarily raises V_N enough to turn FET Q3_N on for a brief period. FET Q3_P remains off. R_{P/N} drops below its quiescent level. This reduces V_T until circuit 26 reduces V_N sufficiently to turn FET Q3_N back off.

Largely the reverse occurs when V_A drops below V_{LL}+V_S. FET Q1_N turns off and FET Q1_P turns on, causing device 22 to switch from its low logic state to its high logic state. V_B goes from V_{LL} up to V_{HH}. In response to this V_B change, circuit 26 temporarily provides V_P at a sufficiently low voltage to turn FET Q3_P on for a short time. FET Q3_N stays off. Consequently, R_{P/N} rises above its quiescent value so as to increase V_T. When circuit 26 subsequently raises V_P to turn off FET Q3_P, V_T drops back down.

The logic circuit in IC 20 also contains an intermediate logic section 28 and output inverter 16. Logic section 28 may perform any of a number of logical functions such as inversion, ANDing, and ORing. Section 28 might also be a non-inverting buffer or simply a direct connection. Depending on how section 28 is configured, it operates on voltage V_B and possibly on other input voltages (not shown) to produce voltage V_C at a value that is logically the same as or inverse to voltage V_B. Inverter 16 consists of FET's Q2_N and Q2_P arranged as described above to produce voltage V_D as the inverse of voltage V_C.

Circuit input voltage V_I and external supply voltages V_{LL} and V_{HH} are supplied respectively to externally accessible terminals T_I, T_L and T_H which are interconnected with the logic circuit via parasitic inductances L_I, L_L and L_H in IC 20 in the same way that these elements are interconnected with the inverting driver in IC 10. The same comments apply to parasitic inductance L_O, capacitance C_O and externally accessible output terminal T_O at which circuit output voltage V_O is provided in IC 20.

Now, look at what happens if voltage V_I is chang-

ing slowly when internal supply line voltage bounce arises in the manner described above. Assume (for example) that section 28 provides a voltage inversion so that V_C is the inverse of V_B. Fig. 4a is a pair of simplified diagrams illustrating voltage variation as a function of time for IC 20 for the case in which V_I rises slowly. Fig. 4b is a corresponding pair of simplified time diagrams for the situation in which V_I falls slowly. In both Figs. 4a and 4b, V_L is initially at V_{LL} while V_H is initially at V_{HH}. Threshold V_T thus starts at V_S.

First consider Fig. 4a which is analogous to Fig. 2. V_I, V_A, V_B and V_O are initially at the values given above for Fig. 2. Capacitor C_O is charged to a high level. As V_I rises, V_A follows closely. Inductance L_I again has no significant effect. When V_A passes V_{LL}+V_S at time t₁, V_B drops rapidly to V_{LL}. In response, hysteresis circuit 24 reduces V_T starting at a time t_{1.5}. The difference between dotted line 30 and the solid line representing V_A-V_T in Fig. 4a indicates the amount of reduction in V_T.

Capacitor C_O starts discharging at time t₂. This produces a positive V_L spike at time t₃ according to the mechanism described above for IC 10. The attendant reduction of the difference between V_H and V_L at t₃ does result in a further V_T reduction beyond that already caused by circuit 24. However, due solely to the V_T reduction produced by circuit 24, V_A-V_L stays above V_T during the positive V_L spike. Capacitor C_O thereby remains discharged so as to substantially inhibit any further internal supply line voltage bounce. Accordingly, no spikes occur in V_B, V_C, V_D and V_O.

At a later time t_{3.5}, V_T automatically returns to V_S. The circuit timing parameters and device values are preferably chosen in such a manner that V_T goes back to V_S before V_I and V_A start to drop in subsequent switching operation.

The falling V_I situation of Fig. 4b is essentially the complement of that of Fig. 4a. In Fig. 4b, hysteresis circuit 24 increases V_T between t_{1.5} and t_{3.5}. The amount of V_T increase is indicated by the difference between dotted line 32 and the solid line labeled V_A-V_T. As the result of the V_T increase, V_A-V_L remains below V_T during the negative V_H spike to prevent further spiking.

Alternatively, section 28 might generate V_C at the same logical value as V_B. If V_I rises slowly, the first supply line spiking occurs on the V_H line as a negative spike followed immediately by a positive spike. Circuit 24 decreases V_T to prevent V_A-V_L from dropping below V_T during the positive V_H spike -- i.e., the second spike in the pair of alternating V_H spikes. The same applies when V_I drops slowly except that the polarities and supply lines are reversed. Since the magnitude of the second spike in each pair of alternating internal supply line spikes is normally slightly less than the magnitude of the first spike, the situation in which V_C and V_B are logically the same is not as critical as when V_C is the inverse of V_B.

Turning to Fig. 5, it depicts a specific embodiment for control circuit 26 in device 22. Circuit 26 here consists of complementary charge-supply FET's Q_{4N} and Q_{4P} , capacitors C1 and C2, and complementary discharge FET's Q_{5N} and Q_{5P} connected as shown in Fig. 5. FET's Q_{4N} and Q_{4P} are arranged as an inverter 34 with their drains connected together to provide a voltage V_E inverse to voltage V_B supplied to their gates.

Circuit 26 in Fig. 5 operates in the following way. When V_B drops from V_{HH} to V_{LL} , FET Q_{4N} turns off and FET Q_{4P} turns on. Current from the V_H line flows through FET Q_{4P} to capacitors C1 and C2. Capacitor C1 provides positive charge to the Q_{3N} gate for a short period of time. During this period, charge also flows to the V_L line by way of a path through FET Q_{5N} which turns on. A competition thus exists between the charging of the Q_{3N} gate by capacitor C1 and the discharging of the Q_{3N} gate through FET Q_{5N} . With appropriate selection for the transistor/capacitor sizes, the average charge rate during the charging period exceeds the average discharge rate by an amount sufficiently great so that voltage V_N rises enough to turn FET Q_{3N} on. Shortly afterwards, the charge on the Q_{3N} gate dissipates sufficiently through FET Q_{5N} to cause FET Q_{3N} to turn back off.

When V_B returns to V_{HH} at a later time, elements Q_{4N} , C2 and Q_{5P} function in a complementary manner to enable FET Q_{3P} to turn on briefly.

Fig. 6 shows a preferred embodiment for control circuit 26. In this case, circuit 26 consists of inverter 34, an inverter 36 that inverts voltage V_E to produce a voltage V_F , an inverter 38 that inverts voltage V_F to produce a voltage V_G , transmission gates 40 and 42, and discharge FET's Q_{5N} and Q_{5P} whose gates receive voltage V_G here. FET Q_{5N} is source-drain connected between the V_L line and the Q_{3N} gate. FET Q_{5P} is similarly source-drain connected between the V_H line and the Q_{3P} gate.

Inverter 36 consists of complementary FET's Q_{6N} and Q_{6P} arranged in the conventional manner shown. Similarly, inverter 38 consists of FET's Q_{7N} and Q_{7P} connected conventionally. Gate 40 is formed with complementary FET's Q_{8N} and Q_{8P} whose gates respectively receive voltages V_F and V_G . FET's Q_{8N} and Q_{8P} have interconnected first source/drain elements connected to the Q_{4N} and Q_{4P} drains and interconnected second source/drain elements connected to the Q_{3N} gate. Gate 42 consists of complementary FET's Q_{9N} and Q_{9P} arranged with regard to the Q_{3P} gate in a manner that is complementary to the arrangement of gate 40 with respect to the Q_{3N} gate.

Circuit 26 in Fig. 6 operates as follows. Assume that V_B is initially at V_{HH} so that FET Q_{4N} is on and FET Q_{4P} is off. V_F is likewise at V_{HH} . V_E and V_G are both at V_{LL} . FET Q_{8N} is on, thereby setting V_N at V_{LL} . FET's Q_{3N} , Q_{5N} and Q_{8P} are all off. When V_B drops to V_{LL} , FET Q_{4N} turns off and FET Q_{4P} turns on. V_E rises to

V_{HH} . During an initial part of the time needed for inverter 36 to drop V_F down to V_{LL} , positive charge from the V_H line flows through FET's Q_{4P} and Q_{8N} to the Q_{3N} gate. V_N increases, enabling FET Q_{8P} to turn on. Although FET Q_{8N} gradually turns off, positive charge from the V_H line now flows through FET's Q_{4P} and Q_{8P} to the Q_{3N} gate to raise V_N further. This continues for the entire time needed for inverter 36 to raise V_G up to V_{HH} . At some point during the charging of the Q_{3N} gate, FET Q_{3N} turns on.

When inverter 38 finally switches, FET Q_{8P} turns off to stop the charging of the Q_{3N} gate. At this point, FET Q_{5N} turns on. It opens a path to the V_L line for discharging the Q_{3N} gate, causing FET Q_{3N} to turn off. Inverters 36 and 38 and FET's Q_{4N} , Q_{9N} , Q_{9P} and Q_{5P} operate in a similar, complementary manner to enable FET Q_{3P} to turn on briefly when V_B later returns to V_{HH} .

If the transmission delay of inverter 36 or 38 is too small to allow enough time to charge the Q_{3N} gate and/or the Q_{3P} gate, a delay element can be placed in series with inverter 36 or 38. The delay element might, for example, consist of a pair of inverters in series.

For the embodiment of Fig. 6, V_{LL} and V_{HH} preferably are 0 volt (ground) and 5 volts. FET's Q_{1N} , Q_{1P} , Q_{3N} , Q_{3P} , Q_{4N} , Q_{4P} , Q_{5N} , Q_{5P} , Q_{6N}/Q_{7N} , Q_{6P}/Q_{7P} , Q_{8N}/Q_{9N} , and Q_{8P}/Q_{9P} have respective channel widths of 100, 270, 50, 100, 20, 50, 1, 5, 5, 10, 10 and 25 microns. The channel length for all of these FET's is preferably 1 micron except for FET Q_{5N} whose channel length is 5 microns.

In some situations, the values at which V_A is provided from an IC preceding IC 20 may not be appropriate for driving FET's Q_{1N} and Q_{1P} directly with V_A so as to achieve a desired quiescent (V_S) value for V_T . Such cases can be handled by inserting a non-inverting buffer in the line leading to the gate of one of FET's Q_{1N} and Q_{1P} . The buffer might, for example consist of a pair of inverters in series. Nonetheless, the gates of FET's Q_{1N} and Q_{1P} are still responsive to V_A . Such an arrangement does not have any particularly significant effect on the dynamic hysteresis.

While the invention has been described with reference to particular embodiments, this description is solely for the purpose of illustration and various modifications could be made. For example, junction FET's could be used instead of insulated-gate FET's. Certain of the enhancement-mode FET's could be replaced with depletion-mode FET's. If dynamic hysteresis is needed only when input V_I rises, FET Q_{3P} and the portions of circuit 26 not used with FET Q_{3N} (for example, FET's Q_{5P} , Q_{9N} and Q_{9P} in Fig. 6) could be deleted. The converse applies if dynamic hysteresis is needed only when V_I falls.

Furthermore, threshold V_T was defined with respect to low supply voltage V_L merely because this is the normal convention. V_T could as well have been

defined with reference to high supply voltage V_H without changing the design, physical operation, or effect of the invention. The only difference is that the polarities relating to V_T would generally have to be reversed in the operational explanation.

Claims

1. An integrated circuit with a switching device comprising, connected between two supply lines (V_{HH} , V_{LL}), a series arrangement (22) of conduction channels of a first ($Q1_n$) and second ($Q1_p$) transistor respectively, said transistors being of mutually opposite conductivity type, receiving the same input voltage (V_A) at their respective control terminals and generating an output voltage at the common node between said transistors, the device comprising at least one additional conduction channel ($Q3_n$, $Q3_p$), in parallel to one of the conduction channels of the first and second transistor ($Q1_n$, $Q1_p$), the device comprising control means (26) responsive to the output voltage, for causing the additional conduction channel ($Q3_n$, $Q3_p$) to conduct when the device switches to make the transistor ($Q1_n$, $Q1_p$) conductive in parallel to which the additional transition channel is placed, characterized in that the control terminals of the first and second transistor ($Q1_n$, $Q1_p$) are interconnected with an externally accessible terminal of the integrated circuit, and in that the control means (26) are arranged for causing the additional conduction channel ($Q3_n$, $Q3_p$) to conduct only for a prescribed period of time after the output voltage of the device has changed logic state.
2. An integrated circuit as claimed in Claim 1, characterized, in that the at least one additional current conduction channel is part of a further transistor ($Q3_n$, $Q3_p$) having the same conductivity type as the transistor ($Q1_n$, $Q1_p$) in parallel to which its conduction channel is placed, the further transistor ($Q3_n$, $Q3_p$) receiving on its control terminal a control voltage generated by said control means (26).
3. An integrated circuit according to Claim 2, wherein the further transistor is referred to as the first further transistor ($Q3_n$) and is in parallel to the conduction channel of the first transistor ($Q1_n$), characterized in that it comprises a second further transistor ($Q3_p$) in parallel to the conduction channel of the second transistor ($Q1_p$) and of the same conductivity type as the second transistor ($Q1_p$), the control means are arranged for causing the conduction channel of the second further transistor ($Q3_p$) to conduct for the prescribed period of time after the output voltage of the device has switched to make the transistor ($Q1_n$, $Q1_p$) conductive in parallel to which the second further transistor ($Q3_p$) is placed.
4. An integrated circuit as claimed in Claim 2 or 3, characterized in that the control means (26) comprises an inverter (34) for charging via an inverter output thereof the control terminal of the further transistor ($Q3_n$, $Q3_p$) via a charging path ($C1$, $C2$, $Q9_n$, $Q9_p$, $Q8_n$, $Q8_p$), said inverter (34) being fed via a junction of the first and second current conduction path, the control means (26) also comprising a discharging element ($Q5_n$, $Q5_p$), connected between the control terminal of the further transistor ($Q3_n$, $Q3_p$) and the relevant supply line (V_H , V_L).
5. An integrated circuit as claimed in Claim 2 or 3, characterized in that the control means (26) comprises a charging path ($C1$, $C2$) between on the one hand a terminal providing a voltage (V_E) inverse to the output voltage (V_B) and on the other hand the control terminal of the further transistor ($Q3_n$, $Q3_p$), and a discharging element ($Q5_n$, $Q5_p$) connected between the control terminal of the further transistor ($Q3_n$, $Q3_p$) and the relevant supply line (V_H , V_L).
6. An integrated circuit as claimed in Claim 4 or 5, characterized in that the charging path comprises a capacitive coupling ($C1$, $C2$) to the control terminal of said further transistor ($Q3_n$, $Q3_p$), whereby said discharging element is one of the following elements: a resistive element, a diode ($Q5_n$, $Q5_p$).
7. An integrated circuit as claimed in Claim 4, wherein said transistors ($Q1_n$, $Q1_p$, $Q3_n$, $Q3_p$) are of the field effect type, characterized in that said charging path comprises a transmission gate comprising a parallel arrangement of conduction channels of a pair of transistors ($Q8_n$, $Q8_p$, $Q9_n$, $Q9_p$) which are of a mutually complementary conductivity type, whereby said discharging element comprises a third transistor ($Q5_n$, $Q5_p$) of the same conductivity type as that of the further transistor ($Q3_n$, $Q3_p$), which third transistor ($Q5_n$, $Q5_p$) has its conduction channel connected between the control terminal of the further transistor ($Q3_n$, $Q3_p$) and the relevant supply line (V_H , V_L), the control terminal of said third transistor ($Q5_n$, $Q5_p$) and the control terminal of the transistor in the transmission gate ($Q8_n$, $Q8_p$, $Q9_n$, $Q9_p$) of the conductivity type opposite to that of the third transistor ($Q5_n$, $Q5_p$) receiving a first control signal of a polarity that is the same as that of the input voltage, the other transistor in the transmission gate



defined with reference to high supply voltage V_H without changing the design, physical operation, or effect of the invention. The only difference is that the polarities relating to V_T would generally have to be reversed in the operational explanation.

Claims

1. An integrated circuit with a switching device comprising, connected between two supply lines (V_{HH} , V_{LL}), a series arrangement (22) of conduction channels of a first ($Q1_n$) and second ($Q1_p$) transistor respectively, said transistors being of mutually opposite conductivity type, receiving the same input voltage (V_A) at their respective control terminals and generating an output voltage at the common node between said transistors, the device comprising at least one additional conduction channel ($Q3_n$, $Q3_p$), in parallel to one of the conduction channels of the first and second transistor ($Q1_n$, $Q1_p$), the device comprising control means (26) responsive to the output voltage, for causing the additional conduction channel ($Q3_n$, $Q3_p$) to conduct when the device switches to make the transistor ($Q1_n$, $Q1_p$) conductive in parallel to which the additional transition channel is placed, characterized in that the control terminals of the first and second transistor ($Q1_n$, $Q1_p$) are interconnected with an externally accessible terminal of the integrated circuit, and in that the control means (26) are arranged for causing the additional conduction channel ($Q3_n$, $Q3_p$) to conduct only for a prescribed period of time after the output voltage of the device has changed logic state.

2. An integrated circuit as claimed in Claim 1, characterized, in that the at least one additional current conduction channel is part of a further transistor ($Q3_n$, $Q3_p$) having the same conductivity type as the transistor ($Q1_n$, $Q1_p$) in parallel to which its conduction channel is placed, the further transistor ($Q3_n$, $Q3_p$) receiving on its control terminal a control voltage generated by said control means (26).

3. An integrated circuit according to Claim 2, wherein the further transistor is referred to as the first further transistor ($Q3_n$) and is in parallel to the conduction channel of the first transistor ($Q1_n$), characterized in that it comprises a second further transistor ($Q3_p$) in parallel to the conduction channel of the second transistor ($Q1_p$) and of the same conductivity type as the second transistor ($Q1_p$), the control means are arranged for causing the conduction channel of the second further transistor ($Q3_p$) to conduct for the prescribed per-

iod of time after the output voltage of the device has switched to make the transistor ($Q1_n$, $Q1_p$) conductive in parallel to which the second further transistor ($Q3_p$) is placed.

4. An integrated circuit as claimed in Claim 2 or 3, characterized in that the control means (26) comprises an inverter (34) for charging via an inverter output thereof the control terminal of the further transistor ($Q3_n$, $Q3_p$) via a charging path ($C1$, $C2$, $Q9_n$, $Q9_p$, $Q8_n$, $Q8_p$), said inverter (34) being fed via a junction of the first and second current conduction path, the control means (26) also comprising a discharging element ($Q5_n$, $Q5_p$), connected between the control terminal of the further transistor ($Q3_n$, $Q3_p$) and the relevant supply line (V_H , V_L).

5. An integrated circuit as claimed in Claim 2 or 3, characterized in that the control means (26) comprises a charging path ($C1$, $C2$) between on the one hand a terminal providing a voltage (V_E) inverse to the output voltage (V_B) and on the other hand the control terminal of the further transistor ($Q3_n$, $Q3_p$), and a discharging element ($Q5_n$, $Q5_p$) connected between the control terminal of the further transistor ($Q3_n$, $Q3_p$) and the relevant supply line (V_H , V_L).

6. An integrated circuit as claimed in Claim 4 or 5, characterized in that the charging path comprises a capacitive coupling ($C1$, $C2$) to the control terminal of said further transistor ($Q3_n$, $Q3_p$), whereby said discharging element is one of the following elements: a resistive element, a diode ($Q5_n$, $Q5_p$).

7. An integrated circuit as claimed in Claim 4, wherein said transistors ($Q1_n$, $Q1_p$, $Q3_n$, $Q3_p$) are of the field effect type, characterized in that said charging path comprises a transmission gate comprising a parallel arrangement of conduction channels of a pair of transistors ($Q8_n$, $Q8_p$, $Q9_n$, $Q9_p$) which are of a mutually complementary conductivity type, whereby said discharging element comprises a third transistor ($Q5_n$, $Q5_p$) of the same conductivity type as that of the further transistor ($Q3_n$, $Q3_p$), which third transistor ($Q5_n$, $Q5_p$) has its conduction channel connected between the control terminal of the further transistor ($Q3_n$, $Q3_p$) and the relevant supply line (V_H , V_L), the control terminal of said third transistor ($Q5_n$, $Q5_p$) and the control terminal of the transistor in the transmission gate ($Q8_n$, $Q8_p$, $Q9_n$, $Q9_p$) of the conductivity type opposite to that of the third transistor ($Q5_n$, $Q5_p$) receiving a first control signal of a polarity that is the same as that of the input voltage, the other transistor in the transmission gate

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(Q8_n, Q8_p, Q9_n, Q9_p) receiving on its control terminal a second control signal of a polarity opposite to that of the input voltage.

8. An integrated circuit as claimed in Claim 7, characterized in that the control means (26) further comprises in addition to said inverter (34), now referred to as the first inverter, a second and a third inverter (36, 38), the second inverter (36) being fed by the first inverter (34) and feeding the third inverter (38), the first control signal being generated on an output terminal of the third inverter (38), the second control signal being generated on the output terminal of the second inverter (36).

Patentansprüche

1. Integrierte Schaltung mit einer Schalteinrichtung, die eine Reihenanordnung (22) von Leitungskanälen eines ersten (Q1_N) beziehungsweise eines zweiten (Q1_P) Transistors von entgegengesetztem Leitfähigkeitstyp zwischen zwei Versorgungsleitungen (V_{HH}, V_{LL}) enthält, die die gleiche Eingangsspannung (V_A) an ihren jeweiligen Steueranschlüssen erhalten und eine Ausgangsspannung an dem gemeinsamen Knotenpunkt zwischen den genannten Transistoren erzeugen, wobei die Einrichtung mindestens einen zusätzlichen Leitungskanal (Q3_N, Q3_P) parallel zu einem der Leitungskanäle des ersten und des zweiten Transistors (Q1_N, Q1_P) umfaßt und auf die Ausgangsspannung reagierende Steuermittel (26) enthält, um den zusätzlichen Leitungskanal (Q3_N, Q3_P) leitend zu machen, wenn die Einrichtung schaltet, damit der Transistor (Q1_N, Q1_P) leitend wird, zu dem der zusätzliche Übergangskanal parallelgeschaltet ist, dadurch gekennzeichnet, daß die Steueranschlüsse des ersten und des zweiten Transistors (Q1_N, Q1_P) mit einem extern zugänglichen Anschluß der integrierten Schaltung verbunden sind, und daß die Steuermittel (26) so angeordnet sind, daß der zusätzliche Leitungskanal (Q3_N, Q3_P) dazu veranlaßt wird, nur für eine vorgegebene Zeitdauer nach der Änderung des Logikzustandes der Ausgangsspannung der Einrichtung zu leiten.
2. Integrierte Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß der mindestens eine zusätzliche Stromleitungskanal ein Teil eines weiteren Transistors (Q3_N, Q3_P) vom gleichen Leitfähigkeitstyp wie der Transistor (Q1_N, Q1_P) ist, zu dem der Leitungskanal parallelgeschaltet ist, wobei der weitere Transistor (Q3_N, Q3_P) an seinem Steueranschluß eine Steuerspannung erhält, die durch die genannten Steuermittel (26) erzeugt

wurde.

3. Integrierte Schaltung nach Anspruch 2, wobei der weitere Transistor als der erste weitere Transistor (Q3_N) bezeichnet wird und parallel zu dem Leitungskanal des ersten Transistors (Q1_N) geschaltet ist, dadurch gekennzeichnet, daß sie einen zweiten weiteren Transistor (Q3_P) parallel zu dem Leitungskanal des zweiten Transistors (Q1_P) vom gleichen Leitfähigkeitstyp wie der zweite Transistor (Q1_P) enthält, wobei die Steuermittel so angeordnet sind, daß der Leitungskanal des zweiten weiteren Transistors (Q3_P) dazu veranlaßt wird, für die vorgegebene Zeitdauer nach der Änderung der Ausgangsspannung der Einrichtung zu leiten, um den Transistor (Q1_N, Q1_P) leitend zu machen, zu dem der zweite weitere Transistor (Q3_P) parallelgeschaltet ist.
4. Integrierte Schaltung nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß die Steuermittel (26) einen Inverter (34) zum Laden des Steueranschlusses des weiteren Transistors (Q3_N, Q3_P) über einen Inverterausgang hiervon und über einen Ladepfad (C1, C2, Q9_N, Q8_N, Q8_P) enthalten, wobei der genannte Inverter (34) über einen Verbindungspunkt des ersten und des zweiten Stromleitungspfades gespeist wird, und wobei die Steuermittel (26) auch ein Entladungselement (Q5_N, Q5_P) enthalten, das zwischen den Steueranschluß des weiteren Transistors (Q3_N, Q3_P) und die entsprechende Versorgungsleitung (V_H, V_L) geschaltet ist.
5. Integrierte Schaltung nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß die Steuermittel (26) einen Ladepfad (C1, C2) zwischen einerseits einem Anschluß zur Lieferung einer Spannung (V_E), die zu der Ausgangsspannung (V_B) invertiert ist, und andererseits dem Steueranschluß des weiteren Transistors (Q3_N, Q3_P) enthalten und ein Entladungselement (Q5_N, Q5_P), das zwischen den Steueranschluß des weiteren Transistors (Q3_N, Q3_P) und die entsprechende Versorgungsleitung (V_H, V_L) geschaltet ist.
6. Integrierte Schaltung nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß der Ladepfad eine kapazitive Kopplung (C1, C2) zu dem Steueranschluß des genannten weiteren Transistors (Q3_N, Q3_P) enthält, wobei das genannte Entladungselement eines der folgenden Elemente ist: ein widerstandsbehaftetes Element, eine Diode (Q5_N, Q5_P).
7. Integrierte Schaltung nach Anspruch 4, wobei die genannten Transistoren (Q1_N, Q1_P, Q3_N, Q3_P) Feldeffekt-Transistoren sind, dadurch gekennzeichnet,



zeichnet, daß der genannte Ladepfad ein Übertragungs-Gatter mit einer Parallelanordnung von Leitungskanälen von einem Paar Transistoren (Q_{8N} , Q_{8P} , Q_{9N} , Q_{9P}) von entgegengesetztem Leitfähigkeitstyp enthält, wobei das genannte Entladungselement einen dritten Transistor (Q_{5N} , Q_{5P}) vom gleichen Leitfähigkeitstyp wie der weitere Transistor (Q_{3N} , Q_{3P}) enthält, wobei der Leitungskanal des dritten Transistors (Q_{5N} , Q_{5P}) zwischen den Steueranschluß des weiteren Transistors (Q_{3N} , Q_{3P}) und die entsprechende Versorgungsleitung (V_H , V_L) geschaltet ist, wobei der Steueranschluß des genannten dritten Transistors (Q_{5N} , Q_{5P}) und der Steueranschluß des Transistors im Übertragungs-Gatter (Q_{8N} , Q_{8P} , Q_{9N} , Q_{9P}) von entgegengesetztem Leitfähigkeitstyp zum dritten Transistor (Q_{5N} , Q_{5P}) ein erstes Steuersignal mit einer Polarität erhalten, die der Polarität der Eingangsspannung entspricht, und wobei der andere Transistor in dem Übertragungs-Gatter (Q_{8N} , Q_{8P} , Q_{9N} , Q_{9P}) an seinem Steueranschluß ein zweites Steuersignal mit zur Eingangsspannung entgegengesetzter Polarität erhält.

8. Integrierte Schaltung nach Anspruch 7, dadurch gekennzeichnet, daß die Steuermittel (26) weiterhin zusätzlich zu dem genannten Inverter (34), jetzt als erster Inverter bezeichnet, einen zweiten und einen dritten Inverter (36, 38) enthalten, wobei der zweite Inverter (36) durch den ersten Inverter (34) gespeist wird und selbst den dritten Inverter (38) speist, wobei das erste Steuersignal an einem Ausgangsanschluß des dritten Inverters (38) erzeugt wird und das zweite Steuersignal an dem Ausgangsanschluß des zweiten Inverters (36) erzeugt wird.

Revendications

1. Circuit intégré avec un dispositif de commutation comprenant, connectés entre deux lignes d'alimentation (V_{HH} , V_{LL}), un montage en série (22) de canaux de conduction respectivement d'un premier transistor (Q_{1N}) et d'un deuxième transistor (Q_{1P}), lesdits transistors étant de types à conductivités mutuellement opposés, recevant la même tension d'entrée (V_A) à leurs bornes de commande respectives et produisant une tension de sortie au noeud commun entre lesdits transistors, le dispositif comprenant au moins un canal de conduction (Q_{3N} , Q_{3P}) additionnel, en parallèle avec l'un des canaux de conduction des premier et deuxième transistors (Q_{1N} , Q_{1P}), le dispositif comprenant des moyens de commande réagissant à la tension de sortie pour provoquer l'état conducteur dudit canal de conduction addi-

tionnel (Q_{3N} , Q_{3P}) lorsque le dispositif effectue une commutation pour rendre conducteur le transistor (Q_{1N} , Q_{1P}) en parallèle avec lequel est placé le canal de transition additionnel, caractérisé en ce que les bornes de commande des premier et deuxième transistors (Q_{1N} , Q_{1P}) sont interconnectées avec une borne, accessible depuis l'extérieur, du circuit intégré, et que les moyens de commande (26) sont agencés pour rendre conducteur le canal de conduction additionnel (Q_{3N} , Q_{3P}), uniquement pendant une période de temps prédéterminée, après que la tension de sortie du dispositif a changé d'état logique.

2. Circuit intégré selon la revendication 1, caractérisé en ce que le au moins un canal de conduction de courant additionnel fait partie d'un transistor supplémentaire (Q_{3N} , Q_{3P}) du même type de conductivité que le transistor (Q_{1N} , Q_{1P}), en parallèle avec lequel son canal de conduction est placé, le transistor supplémentaire (Q_{3N} , Q_{3P}) recevant sur sa borne de commande une tension de commande produite par lesdits moyens de commande (26).
3. Circuit intégré selon la revendication 2, dans lequel le transistor supplémentaire est qualifié de premier transistor supplémentaire (Q_{3N}) et est en parallèle avec le canal de conduction du premier transistor (Q_{1N}), caractérisé en ce qu'il comprend un deuxième transistor supplémentaire (Q_{3P}), en parallèle avec le canal de conduction du deuxième transistor (Q_{1P}) et du même type de conductivité que le deuxième transistor (Q_{1P}), les moyens de commande étant agencés pour provoquer l'état conducteur du canal de conduction du deuxième transistor supplémentaire (Q_{3P}) pendant la période de temps prescrite après que la tension de sortie du dispositif a commuté pour rendre conducteur le transistor (Q_{1N} , Q_{1P}) en parallèle avec lequel est placé le deuxième transistor supplémentaire (Q_{3P}).
4. Circuit intégré selon la revendication 2 ou 3, caractérisé en ce que les moyens de commande (26) comprennent un inverseur (34) destiné à charger, via sa sortie d'inverseur, la borne de commande du transistor supplémentaire (Q_{3N} , Q_{3P}), via un chemin de charge (C_1 , C_2 , Q_{9N} , Q_{9P} , Q_{8N} , Q_{8P}), ledit inverseur (34) étant alimenté via une jonction entre le premier et le deuxième trajet de conduction de courant, les moyens de commande (26) comprenant également un élément de décharge (Q_{5N} , Q_{5P}) relié entre la borne de commande du transistor supplémentaire (Q_{3N} , Q_{3P}) et la ligne d'alimentation (V_H , V_L) concernée.



5. Circuit intégré selon la revendication 2 ou 3, caractérisé en ce que les moyens de commande (26) comprennent un chemin de charge (C1, C2), entre, d'une part, une borne fournissant une tension (V_E) inverse de la tension de sortie (V_B) et, d'autre part, la borne de commande du transistor supplémentaire ($Q3_N$, $Q3_P$) et un élément de décharge ($Q5_N$, $Q5_P$), connecté entre la borne de commande du transistor supplémentaire ($Q3_N$, $Q3_P$) et la ligne d'alimentation (V_H , V_L) concernée.

sortie du deuxième inverseur (36).

6. Circuit intégré selon la revendication 4 ou 5, caractérisé en ce que le chemin de charge comprend un couplage capacitif (C1, C1) à la borne de commande dudit transistor supplémentaire ($Q3_N$, $Q3_P$), de sorte que ledit élément de décharge est l'un des éléments suivants : un élément résistif, une diode ($Q5_N$, $Q5_P$).

7. Circuit intégré selon la revendication 4, dans lequel lesdits transistors ($Q1_N$, $Q1_P$, $Q3_N$, $Q3_P$) sont du type à effet de champ, caractérisé en ce que ledit chemin de charge comprend une porte de transmission comprenant un montage en parallèle des canaux de conduction d'une paire de transistors ($Q8_N$, $Q8_P$, $Q9_N$, $Q9_P$) de types de conductivités mutuellement complémentaires, étant entendu que ledit élément de décharge comprend un troisième transistor ($Q5_N$, $Q5_P$) du même type de conductivité que le transistor supplémentaire ($Q3_N$, $Q3_P$), ledit troisième transistor ($Q5_N$, $Q5_P$) étant connecté par son canal de conduction entre la borne de commande du transistor supplémentaire ($Q3_N$, $Q3_P$) et la ligne d'alimentation (V_H , V_L) concernée, la borne de commande dudit troisième transistor ($Q5_N$, $Q5_P$) et la borne de commande du transistor de la porte de transmission ($Q8_N$, $Q8_P$, $Q9_N$, $Q9_P$), du type de conductivité opposé à celui du troisième transistor ($Q5_N$, $Q5_P$), recevant un premier signal de commande de polarité identique à celle de la tension d'entrée, le transistor supplémentaire, de la porte de transmission ($Q8_N$, $Q8_P$, $Q9_N$, $Q9_P$), recevant sur sa borne de commande un second signal de commande d'une polarité opposée à celle de la tension d'entrée.

8. Circuit intégré selon la revendication 7, caractérisé en ce que le moyen de commande (26) comprend, en plus dudit inverseur (34), appelé ici le premier inverseur, un deuxième et un troisième inverseur (36, 38), le deuxième inverseur (36) étant alimenté par le premier inverseur (34) et alimentant le troisième inverseur (38), le premier signal de commande étant produit sur une borne de sortie du troisième inverseur (38), le deuxième signal de commande étant produit sur la borne de