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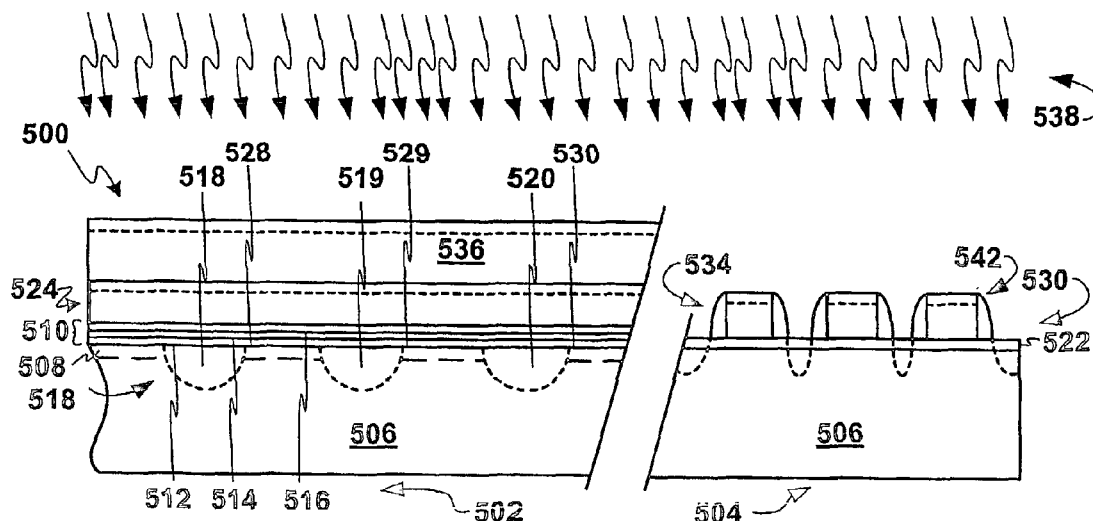
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(54) Title: MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION



(57) Abstract: A method of manufacturing an integrated circuit is provided with a semiconductor substrate (506) having a core region (502) and a periphery region (504). A charge-trapping dielectric layer (510) is deposited in the core region (502), and a gate dielectric layer (522) is deposited in the periphery region (504). Bitlines (518) are formed in the semiconductor substrate (506) in the core region (502) and not in the periphery region (504). A wordline-gate layer (524) is formed and implanted with dopant in the core region (502) and not in the periphery region (504). A wordline (528) and gate (530) are formed. Source/drain junctions are implanted with dopant in the semiconductor substrate (506) around the gate (530), and the gate (530) is implanted with a gate doping implantation in the periphery region (504) and not in the core region (502).

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